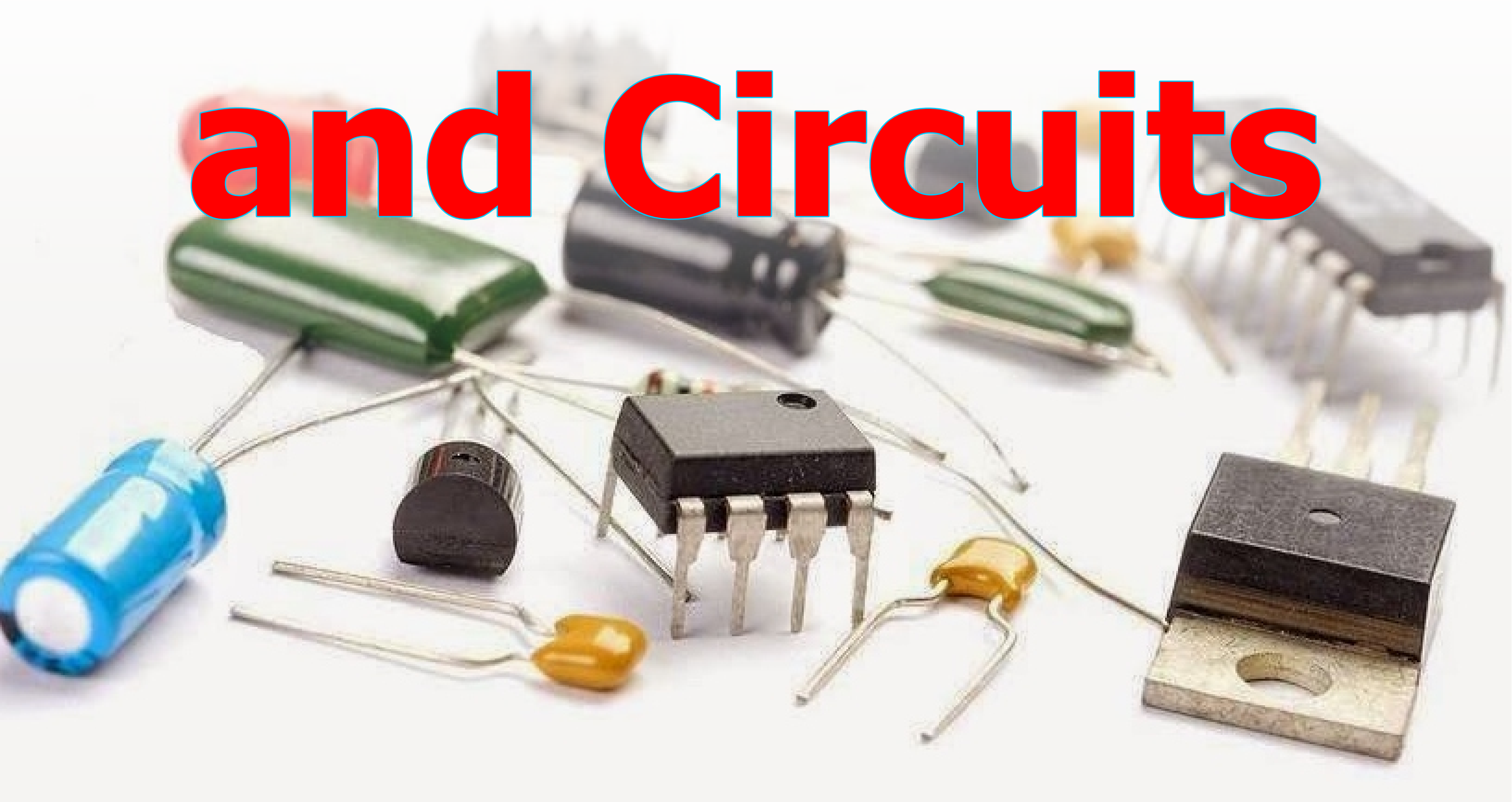
Electronics Device and Circuits



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ELECTRONIC DEVICES

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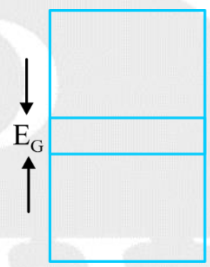
1 SEMICONDUCTOR DEVICE PHYSICS

1.1. Introduction

1.1.1. Energy Gap

Difference between the lower energy level of conduction band E_c and upper energy level of valence band E_v.

$$\boxed{E_G = E_{Go} - B_0 T \text{ eV}}$$



Where, E_{Go} = Energy Gap at 0K

E_G = Energy Gap at T = TK

B_0 = Material constant (eV/K)

T = Temperature in Kelvin

- Energy Gap decrease with increase in the temperature i.e. $\boxed{E_G \propto \frac{1}{\text{Temp}}}$
- For Si Energy Gap is $\boxed{E_{G(T)} = 1.21 - 3.6 \times 10^{-4} T}$
- For Ge Energy Gap is $\boxed{E_{G(T)} = 0.785 - 2.23 \times 10^{-4} T}$

1.1.2. Conductivity

- The current carrying capacity of any material is defined as its conductivity.
- It is the reciprocal of resistivity Unit :– $\frac{1}{\Omega \text{cm}} \rightarrow \frac{℧}{\text{cm}}$
- Conductivity denotes current carrying capacity of material or device

$$\boxed{\text{Conductivity} = \text{carrier conc.} \times \text{charge} \times \text{mobility}}$$

- Conductivity depends on carrier conc, charge and mobility.
- For metal :– $\boxed{\sigma = nq\mu_n}$
- In metal conductivity decrease with increase in temperature.
- In metals as temperature increase, mobility of charge carrier decrease and therefor conductivity decreases.

For semiconductor : $\sigma = nq\mu_n + pq\mu_p$

- In semiconductor, conductivity increases with increase in temperature.
- In a semiconductor, conductivity mainly depends on carrier concentration.
- Semiconductor means by default it is intrinsic semiconductor

1.1.3. Effective Mass

- The effective mass is a quantity that is used to simplify band structure by modeling the behavior of a free particle with the mass.
- Effective mass takes into account the particle mass & also effects due to internal forces
- Consider an electron in an atom

$$\vec{F}_{total} = F_{ext} + F_{internal}$$ where,

$$F_{ext} = m * a$$

and $F_{internal}$ is due to scattering of charges in the structure

- The effective mass is parameter that relates the quantum mechanism results to the classical force equation

$$\frac{1}{\hbar^2}\frac{d^2E}{dK^2} = \frac{2C_1}{\hbar^2} = \frac{1}{m^*}$$

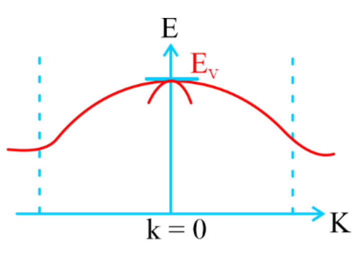
Where, $\hbar$, is plank's constant

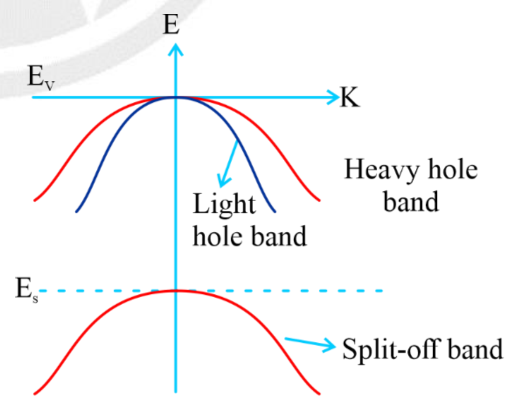
K is wave number

C_1, is constant

m^* is effective mass

- Higher the energy lower will be the effective mass





Where, mp* = effective mass of hole

$$mp^* = \left(m_{lp}^{3/2} + m_{np}^{3/2}\right)^{2/3}$$

mlp = effective mass of light hole

mnp = effective mass of heavy hole

For Si : mlp = 0.16 m_0, mnp = 0.49 m_0

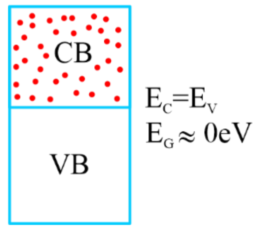
1.1.3. Energy Band Diagrams

Conductors:

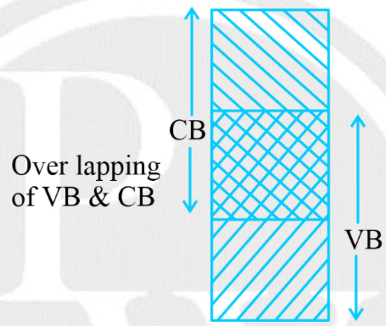
- All metals are very good conductors of current so they allow high flow of current through them.
- In metal current is only due to electrons i.e. metals are unipolar
- In metals free electron conc is independent of temperature

  Where CB = conduction Band and

  VB = valance Band



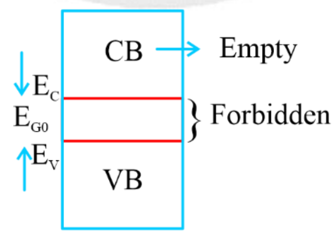
- **At 300 K :**



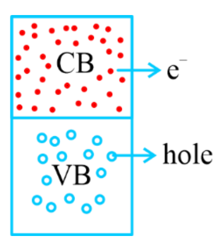
- When temperature is increased then over lapping of CB & VB also increase but there is free carrier concentration available in CB. Hence conductors have Finite amount of conductivity at 300K.

Semi-conductors:

- In semiconductor, the energy gap is small i.e., $E_G \rightarrow 0.7eV$ to $1.5eV$
- At T = 0K free carrier conc. are zero there by conduction band is empty hence conductivity is zero.



- All semiconductors are insulators at 0K.
- At T = 300 K, some covalent bonds are broken & free carriers are generated in CB & holes in VB. So, semiconductor has finite amount of conductivity at T = 300 K.

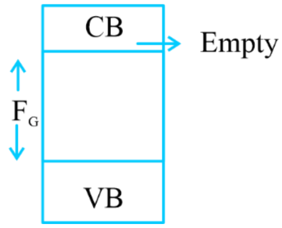


$$E_G \propto \frac{1}{\text{temp}}$$

- Common semiconductor elements are Si, Ge

1.3.4. Insulator

- Due to larger energy gap insulator requires high energy to produce conductivity.
- E_G required is larger
- For ideal insulator conductivity (σ) is zero



1.3.5. Mobility : (μ)

- Moving ability of the charge carriers is called as mobility

$$\boxed{\mu = \frac{V_d}{\vec{E}}}$$

where , V_d = drift velocity

And $\vec{E}$ = field intensity

Unit of μ = $cm^2/V\ sec$

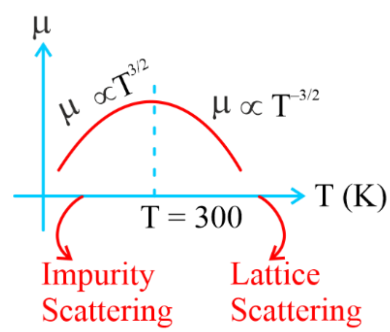
e^- mobility μ_n = $3800\ cm^2 / V\ sec$ for Ge

$1300\ cm^2 / V\ sec$ for Si

Hole mobility μ_p = $1800 cm^2 / V\ sec$ for Ge

$500\ cm^2 / V\ sec$ for Si

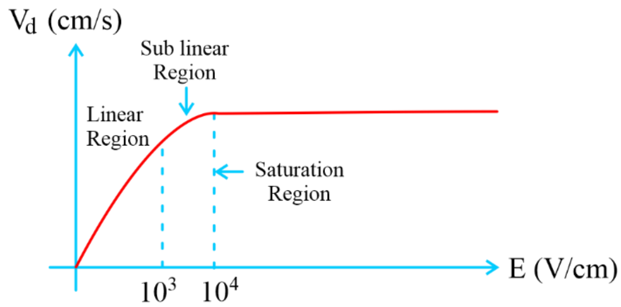
- e^- mobility is always greater then hole mobility so e^-'s can travel faster.
- **Variation of Mobility w.r.t temperature:**



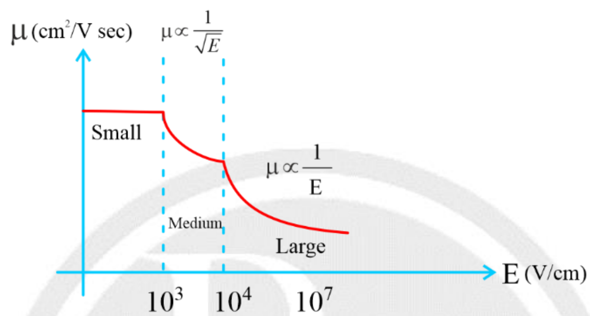
- Impurity scattering takes place till 300 K due to which carriers are generated and the carrier starts moving then drift velocity increases due to which mobility increases.
- Lattice scattering takes place at temp larger than 300 K. In which no. of collisions in e^-s generated increases & relaxation time decrease due to which mobility decreases.
- In general $\boxed{\mu \propto T^{-m}}$

In Ge, $m = 1.66$ for e^- and $m = 2.33$ for hole
In Si. $m = 2.5$ for e^- and $m = 2.7$ for hole

- Variation of drift velocity w.r.t $\vec{E}$ – field :–
- Here V_d (drift velocity) increases linearly then sublinearly then enters into saturation region.



- **Variation of mobility w.r.t $\vec{E}$ field :**



- **For small field Region:** E↑ → Vd↑ (linearly)

  $\uparrow V_d = \mu E \uparrow$

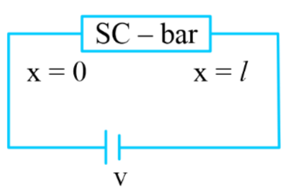
  μ = constant
- Mobility for charge carriers will remain constant
- Drift velocity linearly increases with the field $(\vec{E})$
- For medium field region drift velocity (V_d) increases sublinearly and mobility decreases slowly

$$\boxed{\uparrow V_d = \mu \downarrow E \uparrow}$$

- For high field region drift velocity (V_d) remain constant and mobility decreases as increase of electric field intensity.

$$\text{Constant} \rightarrow \boxed{V_d = \downarrow \mu E \uparrow}$$

1.3.6. Electric field along the length of SC bar :–

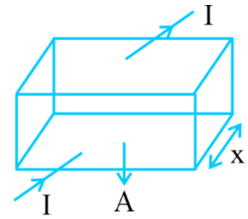


- If length of semiconductor bar is ℓ and applying voltage V then,

$$\boxed{V_{(x)} = V\left(1 - \frac{x}{l}\right)}$$

And $$\boxed{\vec{E} = \frac{V}{\ell}}$$

Current :



- The rate of flow of charge is called current.

$$\boxed{I = \frac{dQ}{dt}}$$

$$\boxed{I = nqV_d A}$$

where, $n \rightarrow$ no. of charge carrier per unit volume (carrier conc)

$V_d \rightarrow$ drift velocity

q = charge

A = Area

1.3.7. Variation of Conductivity w.r.t Temperature

Metal:

- The carrier conc is independent of temp but generally mobility decreases with increase in temp. so conductivity decreases.

$$T\uparrow \rightarrow \mu\downarrow$$

$$\boxed{T\uparrow \rightarrow \sigma\downarrow}$$

Semiconductors:

- In semiconductor as temperature increases, then free e^- concentration in CB & hole conc in VB ↑es by large amount and mobility of e^- & holes decreases wrt temperature by smaller amount. Thus overall the conductivity of SC increases with increases in temperature.

$$\boxed{\uparrow\sigma = \uparrow nq\mu_n + \uparrow pq\mu_p}$$

1.3.8. Resistivity : $\rho(\Omega - m)$

- It is the ability of material to resist the current that passes through it.

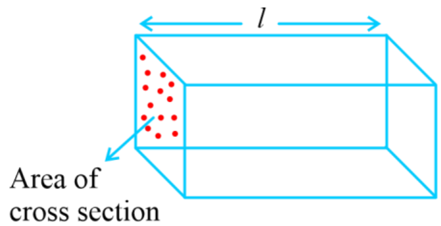
$$\boxed{\rho = \frac{1}{\sigma}}$$

- For metal : $\boxed{\rho = \frac{1}{nq\mu_n}}$

- For semiconductors $\boxed{\rho = \frac{1}{nq\mu_n + pq\mu_p}}$

Resistance : (R) $\boxed{R = \rho\frac{l}{A}}$

Where, ρ = Resistivity



- **For metal :** As increases of temp mobility decreases and Resistivity increases thus overall Resistance increases.
- **For semiconductor :** As increases of temp carrier concentration increases and mobility decreases thus overall resistance decreases.

1.2. Carrier Transport Phenomenon

1.2.1. Drift

- The migration of charge carrier under the influence of external forces which is electric field intensity is called as drift.
- Drift is not natural, It always requires external force.

Diffusion :

- The migration of charge carrier from their higher concentration to lower concentration is called diffusion.
- It is natural process no needs of external forces.
- It occurs due to the concentration gradient.

Drift current Density :– (J_d)

$$\boxed{J_d = \sigma E}$$

- For metal :– In metal drift current density in only due to e^-s

$$\boxed{J_d = nq\mu_n E}$$

- For semiconductor :– In SC drift current density is due to both electrons as well as concentration of holes

$$\boxed{J_d = nq\mu_n E + pq\mu_p E}$$

Where, n = no. of electrons present per cubic meter
p = no. of holes present per cubic meter
q = charge

Diffusion Current Density:

- The diffusion current density depends on diffusion constant or diffusivity
- Diffusion current flows only in semiconductors.
- e^- diffusion current density

where D_n = e^- diffusivity and $\frac{dn}{dx}$ = concentration gradient of e^-

$$\boxed{J_n = +qD_n \frac{dn}{dx}} A/cm^2$$

- Hole diffusion current density

$$\boxed{J_p = -qD_p \frac{dp}{dx}} A/cm^2$$

Where D_p = hole diffusivity

and $\frac{dp}{dx}$ = conc gradient of hole

Total current Density

- The total current density in a semiconductor

$$\boxed{J = J_n + J_p} \text{ A/cm}^2$$

Where Jn = Jn (Diff) + Jn (Drift)

$$\boxed{J_n = qD_n \frac{dn}{dx} + nq\mu_n E} \text{ A/cm}^2$$

$J_p = J_p(\text{drift}) + J_p(\text{Diff})$

$$\boxed{J_p = pq\mu_p E - qD_p \frac{dp}{dx}} \text{ A/cm}^2$$

1.2.2. Einstein's Relation

- It states that the ratio of diffusivity & mobility at a particular temp is always constant

$$\frac{D}{\mu} = \text{constant}$$

$$\boxed{\frac{D}{\mu} = V_T}$$

where V_T = thermal voltage

$$\boxed{V_T = \frac{T}{11600} Volts}$$

where T is temperature, at room temperature, V_T = 25.8mV $\simeq$ 26 mV

1.3. Mass Action Law

It states that, In a semiconductor under thermal equilibrium the product of electrons and holes will be always constant and is given by square of intrinsic concentration.

$$\boxed{np = n_i^2}$$

- This law is mainly used to calculate minority carrier conc.

For n-type semiconductor	For t-type semiconductor
$\boxed{p_n = \frac{n_i^2}{n_n}}$	$\boxed{n_p = \frac{n_i^2}{p_p}}$

Where, $n_n \Longrightarrow$ majority carrier are e⁻s

$p_p \Longrightarrow$ majority carrier are holes

$p_n \Longrightarrow$ minority carrier are holes

n_p = minority carrier are e⁻s

Intrinsic carrier conc : (n_i)

- It is the conc. available in the pure semiconductor at a given temperature

$$\boxed{n = p = n_i}$$

$$\boxed{n_i = \sqrt{N_c N_v}\ e^{-E_{Go}/2kT}}$$

Intrinsic concentration in a semiconductor depends on
(i) Temperature

(ii) Energy Gap

- In Ge intrinsic concentration is more as compare Si due to smaller energy gap at zero kelvin

  For Ge, $n_i = 2.5 \times 10^{13}/\text{cm}^3$

  For Si, $n_i = 1.5 \times 10^{10}$ / cm^3

Classification of semiconductors :

(i) Elemental & compounded type SC
(ii) Direct & Indirect band gap SC
(iii) Intrinsic & Extrinsic SC

1.3.1. Recombination

- In which an e^- after loosing its energy is migrated from conduction band to valence band & acquires a vacancy (hole) in a broken covalent bond & the covalent bond is reformed. This process is called Recombination.

Carrier Life Time (τ)

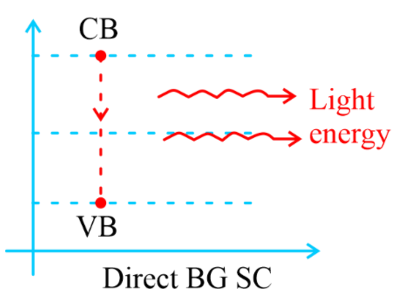
- It is the average lifetime of the charge carriers.
- It is the average time taken from generation to recombination.
- It is two types :

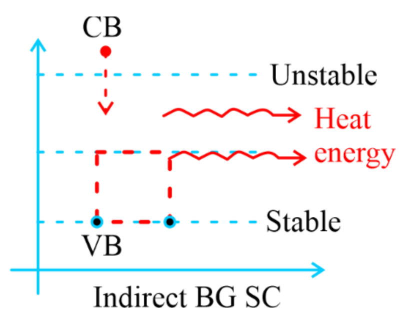
  (i) e^- carrier life time

  (ii) hole carrier life time

Direct and Indirect bandgap SC

- In Indirect bandgap SC, during recombination most of the energy is released in the form of heat because of collision of e^-s to each others.
- In direct band gap SC, during the migration, the value of K is fixed so no. of collision with another e– is very small, so most of energy released in the form of light.

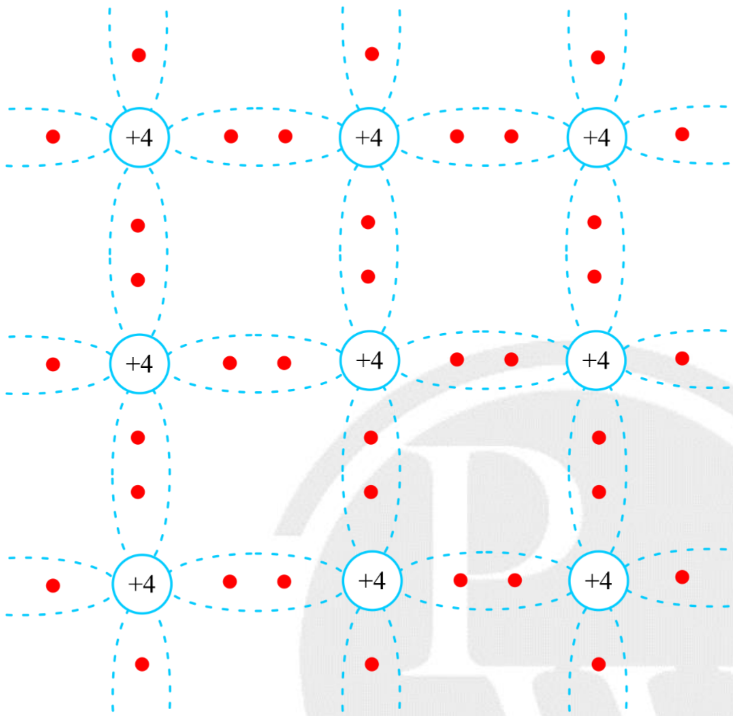


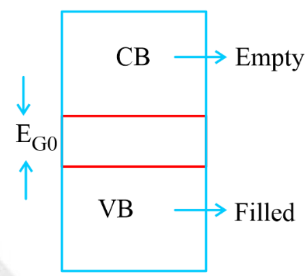


1.3.2. Intrinsic & Extrinsic SC

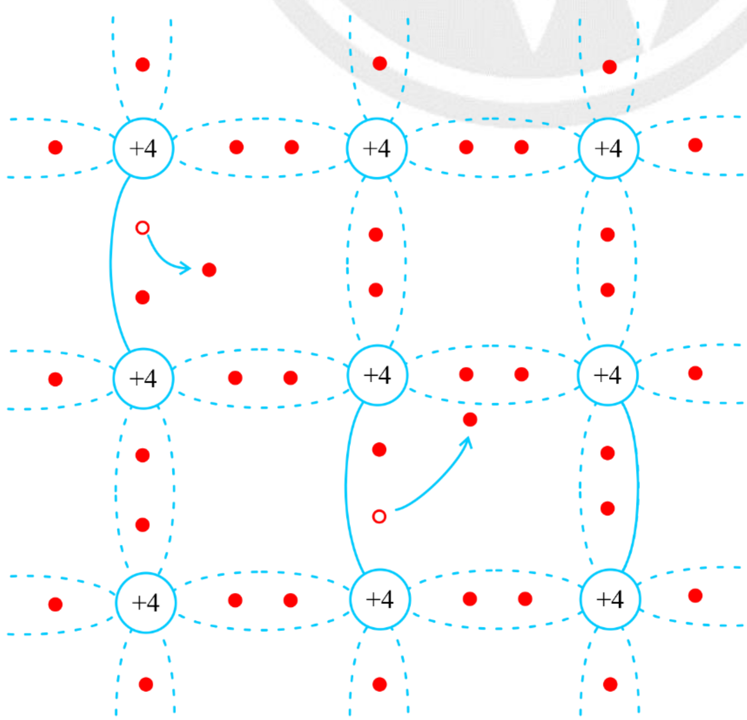
Intrnsic SC

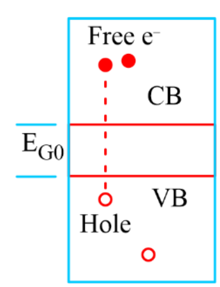
- Also known as pure semiconductor or natural semiconductor or non-degenerate semiconductor
- The maximum no. of valency e⁻s are 8





- In one covalent bond there will be two valency electron
- At 0k all valency e's are imperfect covalent bonding
- Intrinsic semiconductor will act as insulator at 0k.





- When a covalent bond is broken, it will give one e^- & hole (e^- will be jump from VB to CB) and because a free e– and hole will remains in the valency band.
- For intrinsic semiconductor $\boxed{n = p = n_i}$
- Variation in intrinsic concentration w.r.t temperature :–

$$\boxed{\frac{dn_i}{dT} = \frac{1}{T}\left(\frac{E_G}{2KT} + \frac{3}{2}\right)n_i}$$

For Ge at 300 K

$$\boxed{\begin{array}{l} \dfrac{dn_i}{dT} = 0.076\ n_i \text{ at } 300\text{K} \\ \%\dfrac{dn_i}{dT}\Big|_{300K} = 7.6\%\ of\ n_i\ 300\text{K} \end{array}}$$

Note: In Si, n_i increases approximately 8% for 1° rising temp at 300K, As well as the conductivity increases by 8% (approx.) for 1° rising temp

Instrinsic conductivity : (σ_i)

$$\boxed{\sigma_i = n_i q\left(\mu_n + \mu_p\right)}\ ℧/\text{cm}$$

- With increases of temperature intrinsic conductivity will also increases

$$\boxed{\sigma_i \propto T^{3/2}}$$

Intrinsic Resistivity (ρ_i)

It is reciprocal of intrinsic conductivity

$$\rho_i = \frac{1}{\sigma_i}$$

$$\boxed{\rho_i = \frac{1}{n_i q\left[\mu_n + \mu_p\right]}}\ \Omega\ \text{cm}$$

Generation of e^- hole pair :

- The creation of e^- hole pair by Breaking of covalent bond is called generation of EHP (e– - hole pair)

Recombination :

- Pairing of free e– with hole is called as recombination
- During Recombination the free e–s holes will be lost in pair and covalent bond is created

Carrier life time :

- It is the avg lifetime of the charge carriers.
- It is the avg time taken from generation to recombination.

Doping :

- The process of adding impurities to the semiconductor is called doping
- Doping increases the carrier concentration and therefore increases the conductivity
- For an tetravalent atom, there are two types of dopants available

(i) Trivalent dopants : (B, Al, Ga, In) → Valency – 3

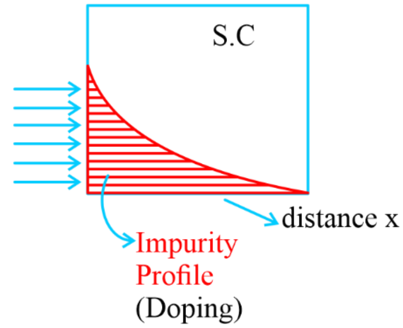
(ii) Pentavalent dopants : (P, As, Sn, Bi) → Valency – 5

Standard Doping concentration :

(i) Moderate Doping → 1 : $[10^6$ to $10^8]$ → P N

(ii) Lightly Doped → 1: 10^{11} → P^- N^-

(iii) Highly/Heavily doped → 1 : 10^3 → P^+ N^+

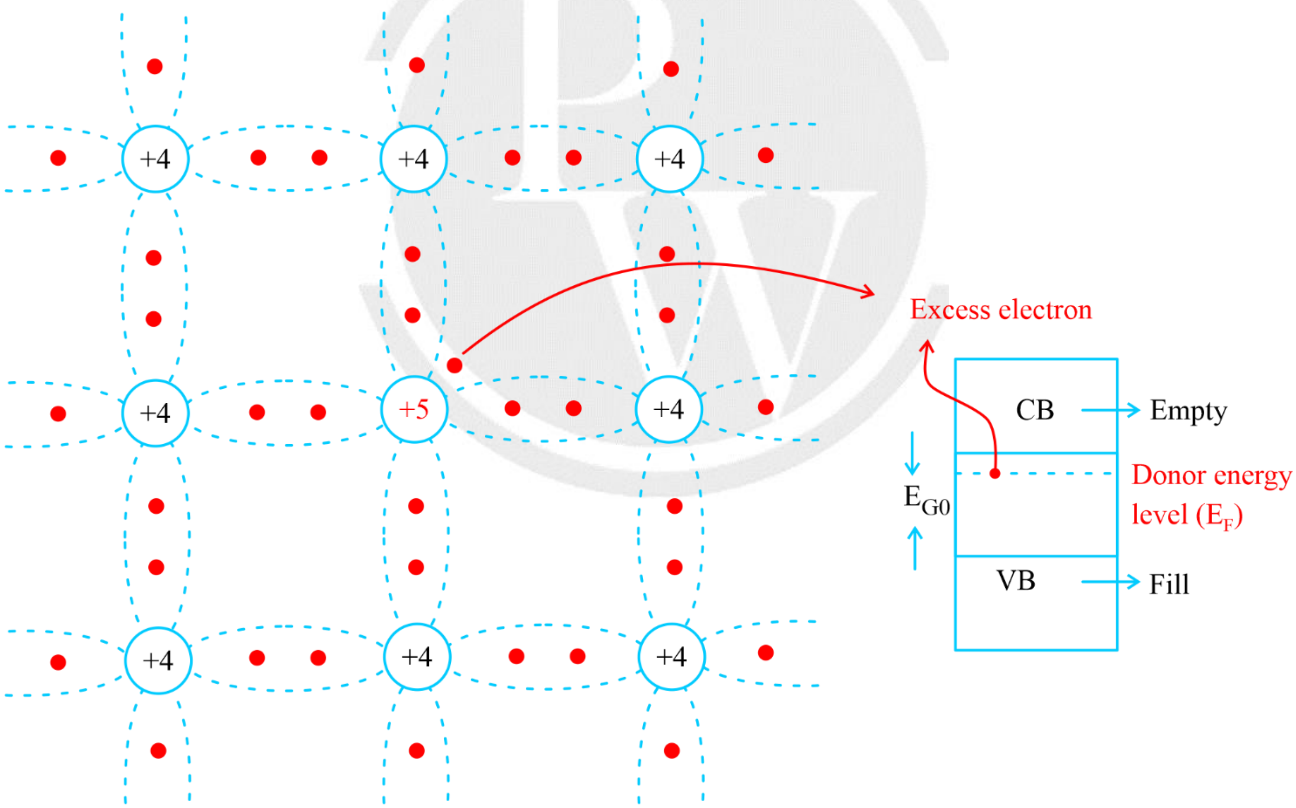


- A highly doped SC with 1 : 10^3 doping is called degenerate SC.
- Non-degenerate SC means moderately doped SC
- The impurity atoms are added to SC are called dopants or impurity profiles

1.3.4. Extrinsic SC

(i) n-type SC

- When pentavalent impurities or donor type impurities are added in the pure SC then it is called as n-type SC
  At T = 0K

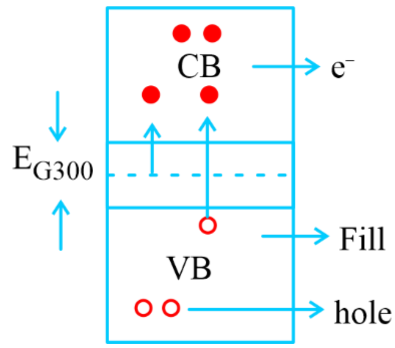


- DONOR energy level is a discrete energy level which is created Just below the conduction band.
- At 0K, the fifth e– of all the impurity atom will be existing in the donor energy level
- N-type semiconductor at 0K will be working as a insulator

$$5^{th}\ e^- = 5 \times 10^{22}\ \text{atoms/cm}^3 \times \frac{1}{10^8}$$

$$= 5 \times 10^{14}\ \text{atoms/cm}^3\ \text{(for Si)}$$

At T = 300 K



- As temperature increases from (0 to 300K) because of that Donor level ionization the 5th e– will be moving from donor energy level into CB and they become free e– and at the same time because of temp large no. of covalent bonds will be broken and (EHP) are generated.
- It overall results in larger e– concentration in CB & hole concentration in VB & the S.C will have finite amount of conductivity

For n-type SC, $N_A = 0$

$$n + N_A = p + N_D$$

$$\boxed{n = p + N_D}$$

For, n-type SC $\boxed{n > p}$

Where $$\boxed{p = \frac{n_i^2}{N_D}}$$

Hence, $$\boxed{n = \frac{N_D + \sqrt{N_D^2 + 4n_i^2}}{2}}$$

- Conductivity :– $\sigma = \sigma_n + \sigma_p$

$$\sigma = nq\mu_n + pq\mu_p$$

σ_p is very small for n-type

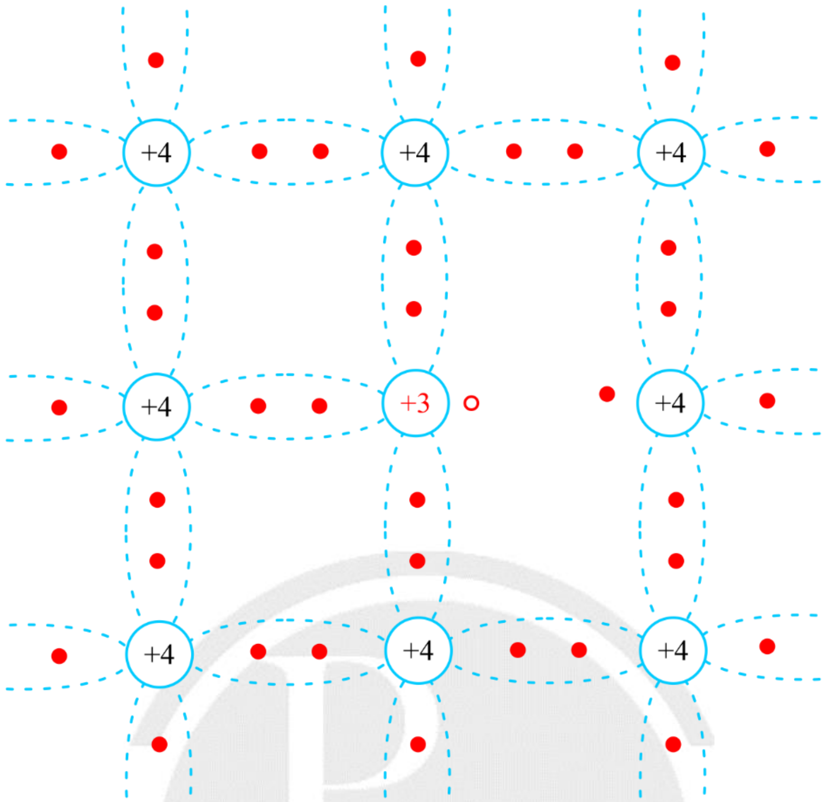
$$\boxed{\sigma = nq\mu_n}$$

If N_D is very large

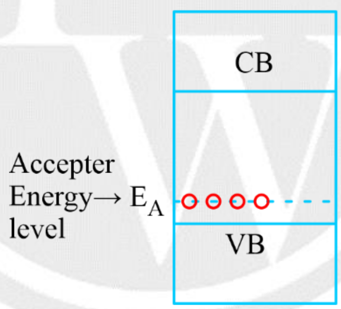
$$\boxed{\sigma = N_D\ q\mu_n}$$

(ii) p-type semi-conductor :

- When trivalent impurities are added into the pure SC then the SC will become p-type

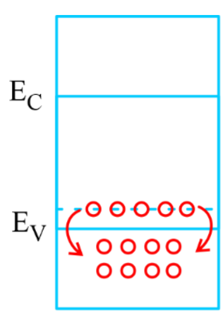


At T = 0 K



- Acceptor energy level is a discreate energy level created Just above the valence band.
- Acceptor energy level denotes energy level of all the trivalent atoms added to the pure semiconductor.
- P-type semiconductor at 0K will be work as a insulator.

At T = 300 K



- At 300K Acceptor level ionization takes place & some covalent bonds are broken therefore, there is finite free e^- concentration in CB & hole concentration in the VB so SC will have finite conductivity at 300 K

For p-type SC :– $N_D = 0$

$$\boxed{p = n + N_A}$$

Where $n = \dfrac{ni^2}{p}$

Hence, $p = \dfrac{N_A + \sqrt{N_A^2 + 4n_i^2}}{2}$

- Conductivity : $\sigma = \sigma_n + \sigma_p$

  Where σ_n is very small for p-type SC

$$\boxed{\sigma = \sigma_p}$$

$$\sigma = pq\mu_p$$

$$\boxed{\sigma = N_A q\mu_p}$$ $\sigma \propto$ doping concentration

Note : Minimum conductivity of extrinsic SC, $\boxed{\sigma_{\min} = 2qn_i\sqrt{\mu_p\mu_n}}$

Doping Ratio or Doping Profile:

It is defined as the ratio of total no. of dopant atoms & total no. of atoms (atomic density) per unit volume in an extrinsic SC.

$$\text{Doping ratio} = \frac{\text{Doping concentration}}{\text{Atomic density}\left(\text{atoms/cm}^3\right)}$$

- $1 : 10^3 \rightarrow$ High Doping
- $1 : (10^6 \text{ to } 10^8) \rightarrow$ Moderate doping
- $1 : (10^{10} \text{ to } 10^{11}) \rightarrow$ Light doping

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2 COMPENSATED SEMICONDUCTORS

2.1. Introduction

Compensated semiconductor:-

- A semiconductor in which both donor & accepter impurities are added are called compensated SC.
- If trivalent atoms are added into n-type SC or pentavalent atoms are added into the p-type SC we get compensated SC.

In an intrinsic semiconductor:-

(i) If $N_A = N_D$ then it is general compensated semiconductor

(ii) If $N_D > N_A$ then it is n-type compensated semiconductor

$$p_n = \frac{n_i^2}{n_n} \Rightarrow p_n = \frac{n_i^2}{N_D - N_A}$$

(iii) If $N_A > N_D$ then it is p-type compensated SC

$$n_p = \frac{n_i^2}{p_p} = \frac{n_i^2}{N_A - N_D}$$

2.1.1. Procedure to calculate majority & minority concentration in the Compensated Semiconductor

(1) N-type – compensated SC

Condition – A:

- If ($N_D >> N_A$) or ($N_D > 10\ N_A$) or ($N_D - N_A$) >> n_i or is not given in the problem then,

minority carrier conc^n $$p_n = \frac{n_i^2}{n_n} \Rightarrow \frac{n_i^2}{N_D - N_A}$$

majority carrier conc^n. $$n_n \simeq N_D$$

Condition – B:

- If N_D is very close to n_i
  $N_D - N_A$ is very close to n_i
  N_D is very close to N_A

then, majority carrier conc^n. (n_n), will be

$$n_n = \frac{N_D - N_A}{2} + \sqrt{\frac{(N_D - N_A)^2}{4} + n_i^2}$$

and minority carrier conc^n will be

$$\boxed{p_n = \frac{n_i^2}{n_n}}$$

Note : Special Case: Let N_D is applied and $N_A = 0$

then $$\boxed{n_n = n = \frac{N_D}{2} + \sqrt{\frac{N_D^2}{4} + n_i^2}}$$

(2) p-type compensated SC :-

Condition A:-

- If $N_A >> N_D$ or $N_A > 10\,N_D$ or $(N_A - N_D) >> n_i$ or n_i is not given
  $p_p \simeq N_A - N_D$

$$\boxed{p_p \sim N_A}$$

and minority carrier conc^n^.

$$\boxed{n_p = \frac{n_i^2}{p_p} = \frac{n_i^2}{N_A - N_D}}$$

Condition B:-

- If N_A is very close to n_i or $(N_A - N_D)$ is very close to n_i or N_A is very close to N_D then, majority carrier conc^n^.

$$\boxed{p_p = \frac{N_A - N_D}{2} + \sqrt{\left(\frac{N_A - N_D}{2}\right)^2 + n_i^2}}$$

Note: Special case:
If N_A is applied & $N_D = 0$

then $$p_p = \boxed{p = \frac{N_A}{2} + \sqrt{\left(\frac{N_A}{2}\right)^2 + n_i^2}}$$

and $$\boxed{n_p = \frac{n_i^2}{p_p}}$$

Carrier Generation & Carrier Recombination:-

Generation is the process in which force electron & holes are generated and Recombination is the process in which electrons & holes are annihilated.

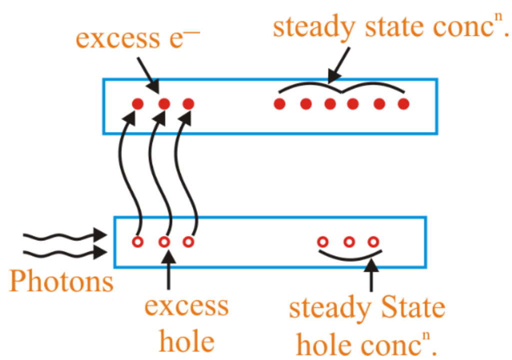
Carrier Generation & Carrier Recombination:

- In thermal equilibrium the conc^n^ of e^- & hole in CB & VB respectively are time independent & mass action law holds and also Recombination process annihilates both the e^- & hole.
- Since the net carrier conc^n^. are independent of time in thermal equilibrium, the rate of e^- and hole generated & the rate of which they annihilates must be equal.
  In thermal equilibrium

$$\boxed{G_{no} = G_{po} = R_{no} = R_{po}}$$

Excess carrier generation & Recombination:-

- When a high energy photons are incident on a SC. e^- in the valence band may be excited to the CB. At the same time, Q hole is also created in the VB. Thus EHP (electron – hole. pair) is generated.



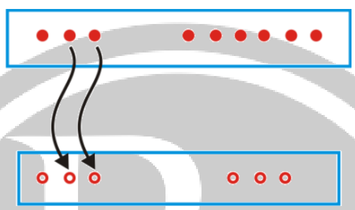
g n´ = g p´

↑

Excess carrier Generation

where gn´ = excess e^- generation rate

gp´ = excess hole generation rate



Excess carrier recombination Rn´ = Rp´

Where, Rn´, Rp´ → Excess e^- & hole recombination rate

Case – I : Source applied for – ∞ to 0

The net rate of change of e^- concentration.

$$\frac{d\,\Delta n(t)}{dt} = D_n \frac{d^2 \Delta n}{dx^2} - \frac{\Delta n}{\tau_n} + G_L$$

Approximation

(i) $p_o >> n_o$ (ii) low level injection

then, $\Delta_n(t) = \Delta_n(o)\, e^{-t/\tau\, n_o}$

For n-type, excess minority carrier concentration.

$$\Delta_p(t) = \Delta_n(o)\, e^{-t/\tau\, p_o}$$

where, τ_{no}, τ_{po} → excess lifetime of e^- & hole.

Recombination rate of excess carrier:

- Recombination rate of excess carrier is equals to negative of net rate of change of excess carrier.
- For p-type, $R_n' = \frac{\Delta n(t)}{\tau_n} = R_p'$
- For n-type, $R_n' = R_p' = \frac{\Delta p(t)}{\tau_p}$

Case – II :

Consider a homogenous n-type SC with zero applied electric field, assume that for t < 0 the SC is in thermal equilibrium & that for t > 0, a uniform generation rate exist in the crystal.

$$\boxed{\Delta p(t) = g'\,\tau_{po}\,(1 - e^{-t/\tau_{po}})}$$

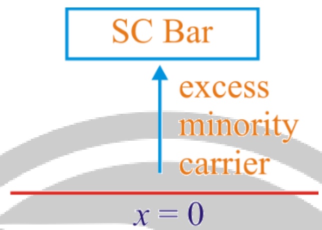
Δ p(t)/max = Δ p(∞)

$$\boxed{\Delta p(t)\,|\,\max = g'\,\tau_{po}}$$

for p-type, $\boxed{\Delta n(t) = g'\tau_{no}\left[1 - e^{-t/\tau_{no}}\right]}$

Case – III : Excess minority carrier concentration with length.

- In this we generate excess carrier at $x = 0$ so for $x < 0$ & $x > 0$
  It will be decayed (diffused).



- For at any 'x' excess minority carrier concentration.

  Let n-type :- $\boxed{\Delta p(x) = \Delta p(o)\, e^{-\frac{x}{Lp}}}$ For ($x \geq 0$)

where, $L_p \rightarrow$ diffusion length for hole

for $x < 0$ $\boxed{\Delta p(x) = \Delta p(o)\, e^{x/Lp}}$

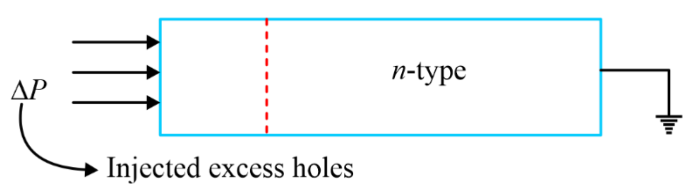
Let p-type $\boxed{\Delta n(x) = \Delta n(o)\, e^{-x/Ln}}$ for ($x \geq 0$)

$\boxed{\Delta n(x) = \Delta n(o)\, e^{x/Ln}}$ for ($x < 0$)

where $L_n \rightarrow$ diffusion length for e^-

Case – II : Dielectric Relaxation time constant:-

- Consider a n-type S.C & let ΔP holes are injected in a portion of that n-type SC. Now we want to find behaviour of those injected excess holes inside the S.C.



$$\boxed{\delta_v(t) = \delta_v(0)e^{-\frac{\sigma}{\varepsilon}t}}$$

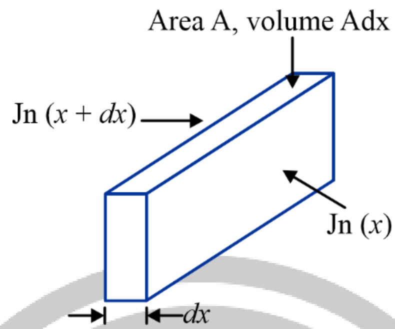
Let $\tau = \dfrac{\in}{\sigma}$ $\Rightarrow \boxed{\delta_v(t) = \delta_v(o)\, e^{-t/\tau}}$

Relation time constant for dielectric

Continuity Equation:

- Continuity equation describes the distribution of electrons and holes when there is excess carrier generation, recombination and carrier movement.
- As per law of conservation of charge, rate of charge of number of e^- inside the semiconductors is equal to no of e^- entering per second minus no. of e^- leaving per second plus no. of e^- generated for second by generation process minus no. of electrons lost per second by recombination process.

- Consider a volume in which carrier flux into/out – of



$$Adx\left(\frac{\partial n}{\partial t}\right) = -\frac{1}{q}\left[J_n(x)\ A - J_n\ (x+dx)A\right] + G_n Adx - R_n\ Adx$$

$$J_n\ (x+dx) = J_n(x) + \frac{\partial J_n(x)}{\partial x}\ dx$$

$$\Rightarrow \quad \frac{\partial n}{\partial t} = \frac{1}{q}\ \frac{\partial .\ J_n(x)}{\partial x} - R_n$$

$$\boxed{\begin{aligned} \frac{\partial n}{\partial t} &= \frac{1}{q}\ \frac{\partial\ J_n(x)}{\partial x} - R_n + G_L \\ \frac{\partial p}{\partial t} &= -\frac{1}{q}\ \frac{\partial\ J_p(x)}{\partial x} - R_p + G_L \end{aligned}}$$

Continuity equation.

- The minority carrier diffusion equations are derived from the continuity equation,

$$\frac{\partial\ \Delta n_p}{\partial t} = D_n\ \frac{\partial^2 \Delta n_p}{\partial x^2} - R_n + G_L$$

$$\frac{\partial\ \Delta\ p_n}{\partial t} = D_p\ \frac{\partial^2\ \Delta p_n}{\partial x^2} - R_p + G_L$$

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3 FERMI LEVELS AND HEAT MEASUREMENT

3.1. Fermi Characteristic

(a) Fermi-Dirac Distribution: $f(E)$

$$f(E)=\frac{1}{1+e^{\frac{E-E_F}{KT}}}$$

Where, E = Energy possessed by the e^- in eV
K = Boltzmann constant
E_F = Fermi energy level

- Indicates the probability of existing e^- in a given energy state
- It is also called as fermi – Dirac probability function
- At T = 0 K

(i) $E > E_F,\ f(E)=\frac{1}{1+e^{+\infty}}=\frac{1}{1+\infty}=0$, this indicates no e^- are available in the SC with energy $E > E_f$

(ii) $E < E_F,\ f(E)=\frac{1}{1+e^{-\infty}}=\frac{1}{1+0}=1$

Here probability is 1 it indicates at T = 0 K, elements are available in the semiconductor with energies $E < E_f$

- At T ≠ 0 K

$$E = E_F,\quad f(E)=\frac{1}{1+e^0}=\frac{1}{2}\text{ or }50\%$$

- Fermi level is the characteristic level with 50% probability of being filled if no forbidden band exist
- For metal f(E) will be 1
- For SC if probability of e^- existing f(E) then probability of hole existing in SC will be [1 – f(E)]

(b) Fermi Energy (E_F)

- Fermi energy is defined as the maximum energy possessed by the e^- at 0K

$$E_F = \text{Max kinetic Energy}$$

$$E_F=\frac{1}{2}mv_{\max}^2$$

Where, m = rest mass of e^- = 9.1×10^{-31} kg

and $$V_{max}=\sqrt{\frac{2E_F}{m}}\text{ m/s}$$

- Fermi energy is also defined as the energy possessed by fastest moving e^- at 0K

(c) Fermi Energy Level in Intrinsic semiconductor (E_{Fi})

- In Intrinsic SC, $n = p = n_i$

  Where, $n = N_c \cdot e^{\frac{-(E_c - E_{Fi})}{KT}}$

  $p = N_v \cdot e^{\frac{-(E_{Fi} - E_v)}{KT}}$

  $$N_c \cdot e^{\frac{-(E_c - E_{Fi})}{KT}} = N_v \cdot e^{\frac{-(E_{Fi} - E_v)}{KT}}$$

  by solving

  $$E_{Fi} = \frac{E_c + E_v}{2} + \frac{KT}{2} \ln\left(\frac{N_v}{N_c}\right)$$

  Where $\frac{E_c + E_v}{2} = E_{\text{midgap}}$

  and $N_v \propto (m_p^*)^{3/2}$

  $N_c \propto (m_n^*)^{3/2}$

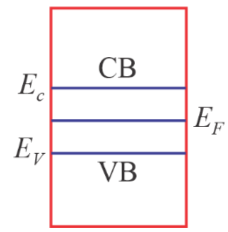
  $$E_{Fi} = E_{\text{midgap}} + \frac{3}{4} KT \ \ln\left(\frac{m_p^*}{m_n^*}\right)$$

- If $m_p^* = m_n^*$ then $E_{Fi} = E_{\text{midgap}}$, Intrinsic fermi – energy level lies at the midgap
- If $m_p^* > m_n^*$ then $E_{Fi} > E_{\text{midgap}}$, E_{fi} lies just above midgap
- If $m_p^* < m_n^*$ then $E_{Fi} < E_{\text{midgap}}$, E_{fi} lies just below the midgap

Effect of Temperature:

1. AT T = 0 K, In intrinsic SC at 0 K, fermi level is existing at the centre of energy gap

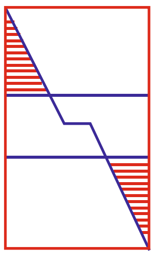
   $$E_F = \frac{E_c + E_c}{2}$$

   Note : Fermi level will be exactly at the centre of energy gap
   (i) $m_n^* = m_p^*$
   (ii) $N_c = N_v$
   (iii) At T = 0 K

2. AT T = 300 K, In intrinsic semiconductor at room temperature, the fermi level will be passing through centre of energy gap.

   $$E_F = \frac{E_c + E_v}{2} - \frac{KT}{2} \log_e\left(\frac{N_c}{N_v}\right)$$

   here e^- conc. = hole conc.

(d) Fermi level in *n*–type semiconductor (E_{Fn}) :

- In n-type SC : $n \simeq N_D$

$$n \simeq N_D = N_c \cdot e^{-\frac{(E_c - E_{Fn})}{KT}}$$

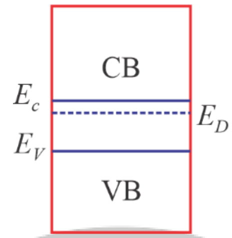
$$E_{Fn} - Ec = \text{KT}\ln\left(\frac{N_D}{N_C}\right)$$

- It indicates the position of fermi level below the conduction band
- In n-type semiconductor, fermi level is a function of temperature and doping conc.

Effect of Temperature:

(i) At T = 0 K, $\boxed{E_F = E_c}$ E_f is coincides with the edge of conduction band.

⇒ Donor energy level is always nearer to conduction band as compare to centre



(ii) At T = 300 K

- At room temperature, in n-type semiconductor fermi level exist just below CB Energy level
- At T = 0 K

  Semiconductor is non-degenerated i.e. ($N_D < N_C$)

  Here $E_{Fn} < E_c$, means fermi level lies below CB

  If semiconductor is degenerate, i.e. ($N_D > N_C$) here $E_{Fn} > E_c$, mean fermi level lies in conduction band.

(e) Effect of Doping :

- Shift in position of E_F due to Doping
- Shift in position of E_F w.r.t to E_{Fi}

$$\phi_n \text{ (Shift)} = +KT\ell n\frac{N_D}{n_i} eV$$

(f) Fermi -Energy level in p-type semiconductor (E_{Fp})

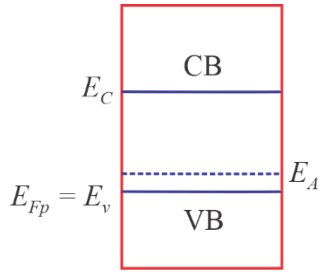
- on p-type SC, $p \simeq N_A$

$$p = N_A = N_v e^{\frac{-(E_{Fp}-E_v)}{KT}}$$

$$E_{Fp} = E_v + KT\ell n \frac{N_v}{N_A}$$

- It indicates the position of fermi level above the valence band in the p-type semiconductor
- Fermi level is a function of temperature and doping
- At T = 0 K, $\boxed{E_{Fp} = E_v}$, E_{Fp} coincides with the edge of VB

→ At 0 K, carrier conc. Are zero and therefore $\sigma = 0$, so p-type SC at 0 K behave as insulator.



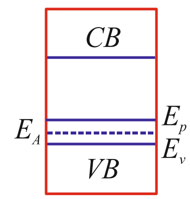
- At T = 300 K :

  $E_{Fp} = E_v + KT \log_e \dfrac{N_v}{N_A}$, In p-type semiconductor at 300 K fermi level exist just above the accepter energy level

at T > 0 K, if $N_A < N_v$ means $E_{Fp} > E_v$ here fermi energy level lies above VB (Non degenerated SC)

If $N_A > N_v$ means $E_{Fp} < E_v$ (generated SC)

Here fermi energy level lies above VB.



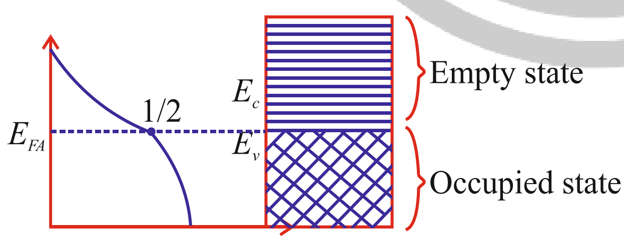
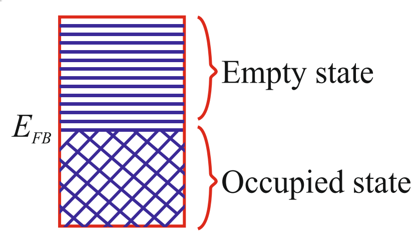
Effect of Doping :

- In p-type semiconductor as doping (N_A) increases then E_F moves towards the VB.
- As E_F moves away from the centre energy gap so σ increases with doping
- Shift in the position of E_F due to doping

$$\text{Shift} = -KT\,\ell n \frac{N_A}{n_i}\,\text{eV}$$

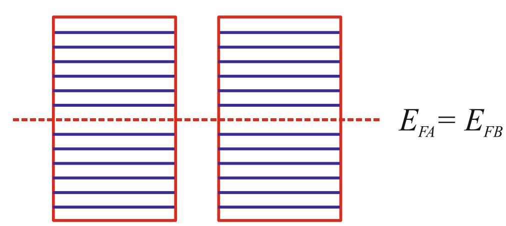
(g) Effect on fermi level when two different SC brought together:

In thermal equilibrium, the fermi energy level is constant through the system

Consider a S·C A Whose $e^{\ominus}$ are distributes in the energy state of an allowed band. 	**Consider a S·C B** Whose $e^{\ominus}$ are distributes are the energy state of an allowed band. 

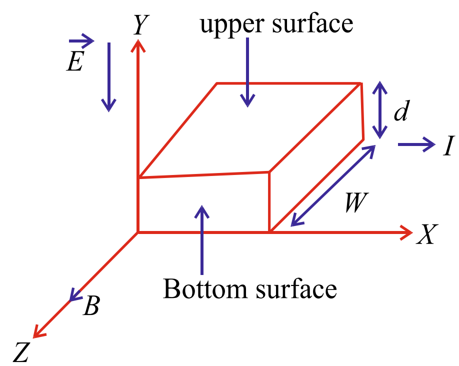
- It there two material are brought togethers into intimate contact then the $e^{\ominus}$ in *n*-type system will tend to seek the lowest possible energy level.
- In those above case, $e^{\ominus}$ will flow from material A to lowest energy state of material and until thermal equilibrium reach.
- Thermal equilibrium is only reached when distribution of electron is a function of energy is same in both material. It occour when fermi level will equal in both system

  Let $E_{FA} > E_{FB}$, In thermal equilibrium



3.2. Hall Effect

It states that if a specimen (metal or SC) currying the current I is placed in transverse magnetic field and an electric field intensity E is induces in perpendicular direction of both ‘I’ and ‘B’



where, w = width of specimen

d = height of specimen

current in X – direction $\Rightarrow I_X$

Magnetic field in Z – direction = B_Z

Field intensity in Y – direction = E_Y

- The specimen must be square shape or rectangular shape.
- From the hall effect we can identify.

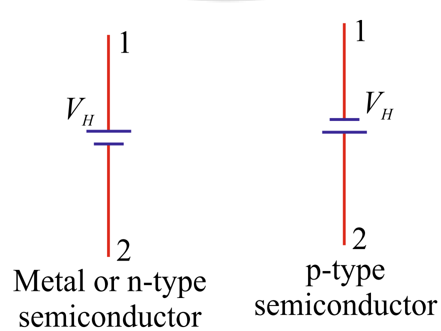
I. Whether the given specimen is a metal or SC (n-type or P-type)

II. The carrier concern in the specimen.

III. The mobility of charge caries.

IV. Magnetic field intensity ‘H’

V. To measure the signal power in the electromagnetic wave.



- Hall voltage is induced voltage.
- Electric field intensity.

$$\boxed{|E| = \frac{|V_H|}{d}} \text{ V/m}$$

Hall voltage V_H:

$$\boxed{V_H = Ed} \text{ volt}$$

$$V_H = \frac{BI}{\rho w}$$

where, ρ is charge density.

$$\boxed{\frac{1}{\rho} = R_H}$$

where, R_H is hall coefficient.

$$\boxed{V_H = \frac{BI\,R_H}{W}} \; volt$$

Where, B → applied magnetic field
W → width of specimen

- By hall experiment, mobility is given by

$$\boxed{\mu = \frac{8}{3\pi}\sigma R_H}$$

Where, μ = mobility of charge carriers
σ = conductivity of metrical

Application:

I. Magnetic field meter.
II. Hall effect multiplier.

Hall voltage depends upon carrier concentration:

In metal, V_H = –ve

In n-type semiconductor, V_H = –ve

In P-type semiconductor, V_H = +ve

For intrinsic semiconductor, $V_H = 0$

Note : Charge density (ρ) = charge × carrier conc. C/m^3

Hall coefficient (R_H):

$$\boxed{R_H = \frac{1}{\rho} = \frac{1}{\text{charge} \times \text{carrier conc.}}} \; m^3/c$$

- In metal and n-type semiconductor R_H = –ve
- In p-type SC, R_H = +ve
- In intrinsic SC, R_H is very large
- In intrinsic semiconductor carrier concentration are very small and so Hall coefficient will by very large

$$\mu = \sigma R_H$$

So, $$R_H \propto \frac{\mu}{\sigma}$$

Since, $$V_H \propto R_H$$

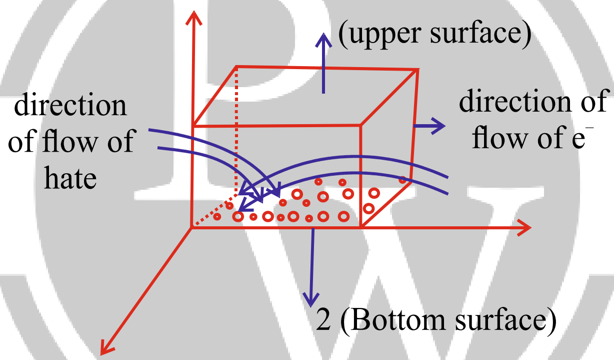
Since, $V_H \propto \frac{1}{\sigma}$

- In metal V_H is small because of in metal σ is very large.
- In semiconductor V_H is large because of semiconductor σ is small.
- In extrinsic SC, R_H is independent of temperature.

$$R_H = \frac{1}{q \times \text{carrier concentration}}$$

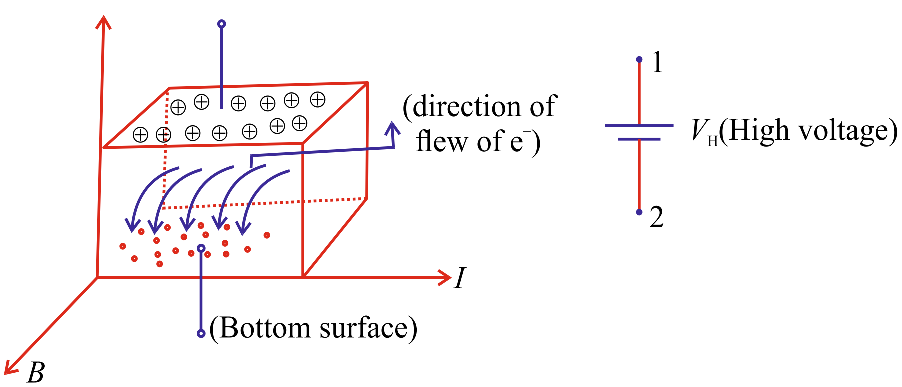
- $R_H = \frac{V_H W}{BI}$, since all parameter are constant so, hall coefficient is independent of temperature.
- $R_H = \frac{\mu}{\sigma}$, in intrinsic semiconductor, hall coefficient decreases with in temperature.
- $R_H = \frac{1}{q \times corrier\ conc}$, As in intrinsic semiconductor for carrier conc. increases with temperature so R_H decreases with temperature.

Hall coefficient (R_H):



- Increases of intrinsic SC, current will be produces by both e⁻ and holes because of no majority and minority. Increase of intrinsic SC due to which both change carrier will have magnetic force in (-gy) dissection deposited on bottom surface.

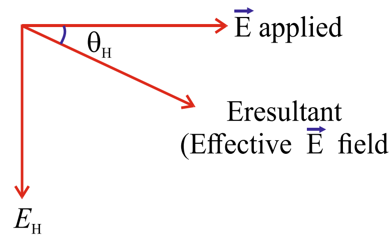
For n-type SC:



- For n-type SC bottom plate will be positively charge.

Half angle:

- Hall angle is defined as the angle made by the resultant $\vec{E}$ field with applied $\vec{F}$ field.



$$\tan(\theta_H) = \frac{E_H}{E_{applied}}$$

$$E_H = \frac{V_H}{d},\ J = \frac{I}{A} = E_{applied}.\sigma$$

So,

$$E_{applied} = \frac{I}{\sigma A}$$

$$\tan(\theta_H) = \frac{VH}{d.I} \times \sigma \times A$$

$$\tan(\theta_H) = \frac{R_H.IB \times \sigma A}{w.d \times I}$$

$$\tan(\theta_H) = R_H \times B \times \frac{\mu}{R_H}$$

$$\boxed{\theta_H = \tan^{-1}(B\mu)}$$

4 PN JUNCTION

4.1. PN Junction

(a) PN Junction

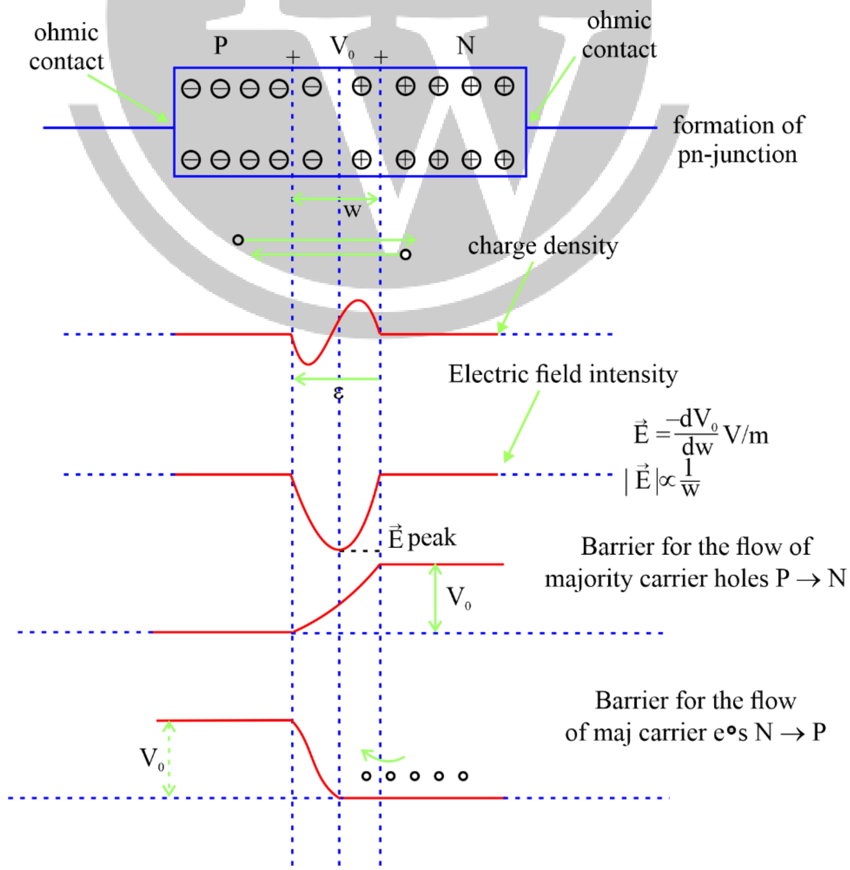
- A pn – junction can be formed only when a bonding force is created in between p – type and n – type semiconductor
- Modern diodes are fabricated with using any one of the following methods

  (a) Alloy – junction method

  (b) Diffusion method

  (c) Grown junction technique

  (d) Epitaxial method



For Ge diode, V_0 = 0.1 v to 0.5 V

Typical value – 0.2 V

For Si diode, V_0 = 0.6 v to 0.98 v and typical value = 0.7 v

- Depletion layer is called as space charge region or transition region
- Depletion layer is created due to diffusion of majority carrier across junction
- In depletion layer mobile charge carrier are zero and contains immobile charge carrier
- Contains large no. of covalent bonds & Ions
- Depletion layer consist of (–ve) charges and positive charges on either side of the junction
- Depletion region not oppose minority carrier in crossing the junction

$$w \propto \frac{1}{\sqrt{\text{Doping concentration}}}$$

Where , w is width of depletion region

- By increasing doping concentration on both sides of the p – n junction or on one side of the junction, the width of depletion region will be reduced
- In Pn junction , v_0 is
  - Contact potential
  - Barrier potential
  - Diffusion voltage
  - Built in voltage
- In any type of PN junction field intensity is always directed from n – side to p – side
- In pn – junction field intensity is always maximum at the junction

Equation for width of depletion layer (ω)

$$w = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)v_0}$$

Where, ε = permittivity in F/m ⇒ ($\varepsilon = \varepsilon_0\varepsilon_r$)

ε_0 = permittivity in free space

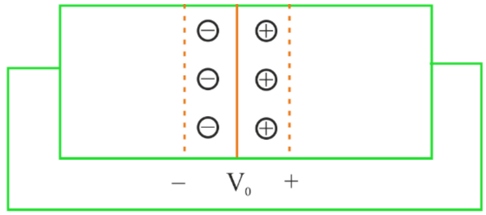
And ε_r = Absolute permittivity

Note: $\varepsilon_0 = 8.84 \times 10^{-12}$ F/m

$\varepsilon_r(\text{Si}) = 11.7$, $\varepsilon_r(\text{Ge}) = 16$

$\varepsilon = 11.7\ \varepsilon_0 = 8.85 \times 10^{-14}$ F/cm

Equation for contact potential of PN junction diode



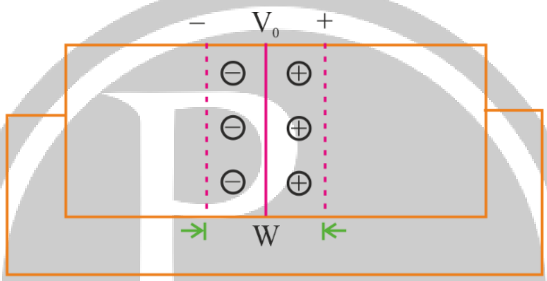
S.C. conditon

$$V_0 = V_{bi}$$

$$V_0 = V_T \ell n \frac{N_A N_D}{n_i^2}$$

- Contact potential is always (+v) for p – n junction diode
- Contact potential decreases with the temperature for increase in 1°C, v_0 is decrease by 2.5 mV

Equation for maximum field intensity in the p – n junction



unbiased

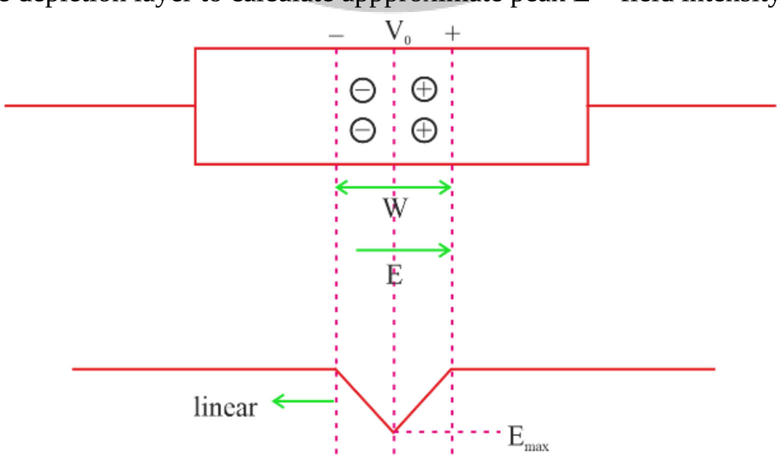
Maximum intensity is given by poison's equation

$$\vec{E}_{max} \text{ or } E_{peak} = \frac{-q}{\varepsilon} w_N N_D = -\frac{q}{\varepsilon} w_p N_A$$

When w_n or x_n is width of n – side depletion layer and w_p or x_p is width of p – side depletion layer

Special Case:

Assuming $\vec{E}$ is linear with the depletion layer to calculate appproximate peak E – field intensity



$$E_{max} = \frac{-v_0}{W/2} = \frac{-2v_0}{W} \text{ v/m}$$

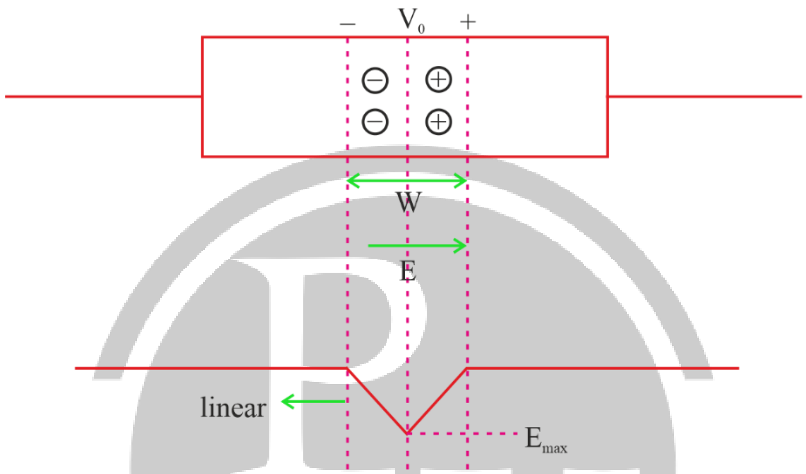
Equation for width of depletion layer (w) :

$$\text{Using } E_{max} = \frac{-q}{\varepsilon} w_n N_D \text{ or } -\frac{q}{\varepsilon} w_p N_A$$

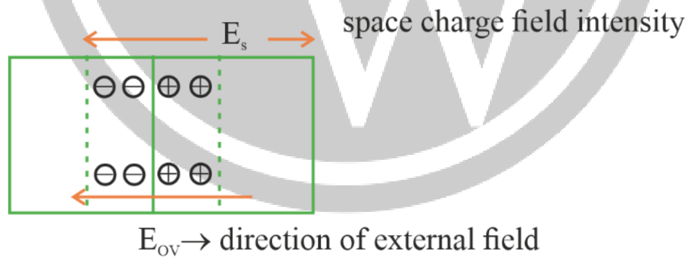
$$w_n = \frac{WN_A}{N_A + N_D} \qquad w_p = \frac{WN_D}{N_A + N_D}$$

$$w = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_0}$$

Current components in p – n junction diode



4.2. Law of Electrical Neutrality



In + qA w_pN_P and –qA w_nWD_D (Coulomb)

The charge density in the depletion region of N side and P side are $+qw_nN_D$ C/m^2 and – qw_pN_A C/m^2

Or

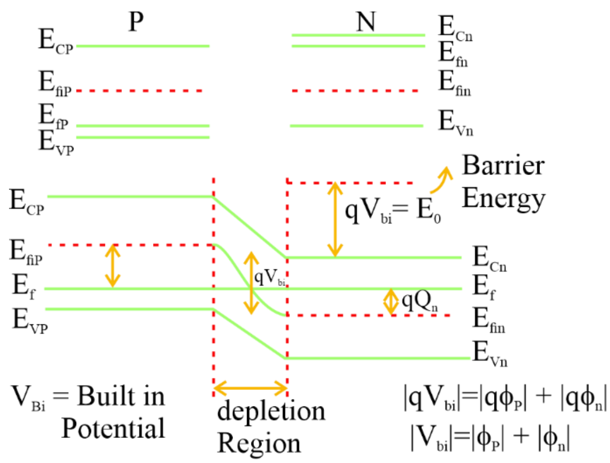
$$w_pN_A = w_nN_D$$

or,
$$\frac{w_p}{w_n} = \frac{N_D}{N_A}$$

Note :

- Ratio of depletion layer width of p – side & n – side depends on their doping concentration called charge equality equation
- Depletion layer will penetrate more into lightly doped region
- In a p – j junction if doping concentration are 10 : 1 then their depletion layer will be 1 : 10 ratio

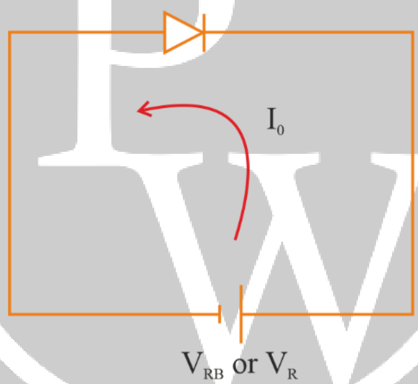
Energy Band diagram



Built in potential, $$V_{bi} = \frac{KT}{q}\ell n\left(\frac{N_A N_D}{n_i^2}\right)$$

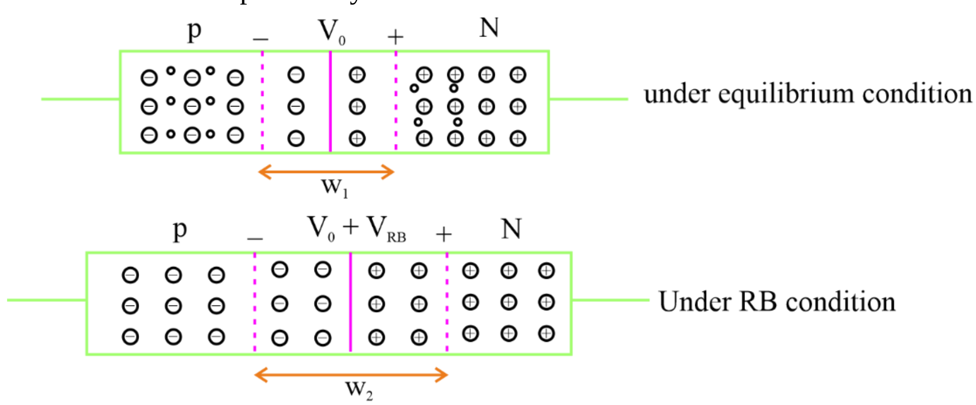
And Barrier energy $$E_0 = qV_{bi} = KT\ell n\left(\frac{N_A N_D}{n_i^2}\right)$$

Reverse Bias : or blocking bias



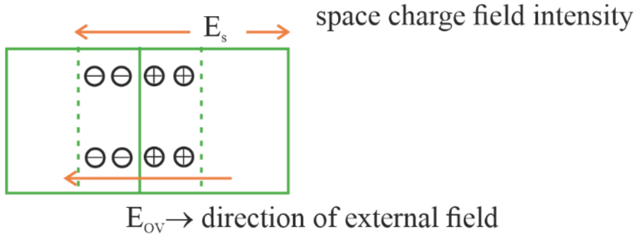
If we apply 0 potential difference between p & N region such that the n – side is at higher potential or +ve potential as compared to p – side, then the applied bias is called as reverse bias

Under the reverse bias the width of the depletion layer is increased



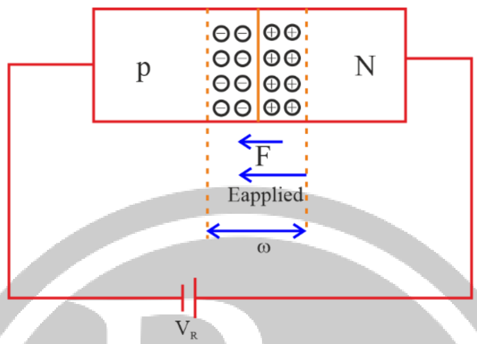
Here , ($w_2 > w_1$)

Here majority carriers of p – n junction will be moving away from the junction there by the region of immobile charges ↑ es. That width of depletion layer is increased



- Both have same direction E_s & E_{ov}
- Under RB, the barrier voltage is increase by $|V_{RB}|$

4.2.1 Space Charge width & Electric Field



Where, $\vec{E} = \vec{E}$ Field that exist in depletion region already

On space charge region

$$\vec{E}_{net} = \vec{E} + \vec{E}_{app}$$

The $\vec{E}$ field originates from the +ve charges & terminates on – ve charges, this means the no. of +ve & –ve charge must ↑ ses if $\vec{E}$ field increases

w ↑ es with an increasing reverse voltage V_R

Here, $V_{total} = V_{bi} + V_R$

(i) $W = \sqrt{\frac{2\varepsilon}{q}(V_{bi}+V_R)\frac{N_A+N_D}{N_A N_D}}$

(ii) $x_n = \sqrt{\frac{2\varepsilon}{q}(V_{bi}+V_R)\frac{N_A}{N_D}\cdot\frac{1}{(N_A+N_D)}}$

(iii) $x_P = \sqrt{\frac{2\varepsilon}{q}(V_{bi}+V_R)\frac{N_D}{N_A}\cdot\frac{1}{(N_A+N_D)}}$

$\vec{E}$ field in depletion region

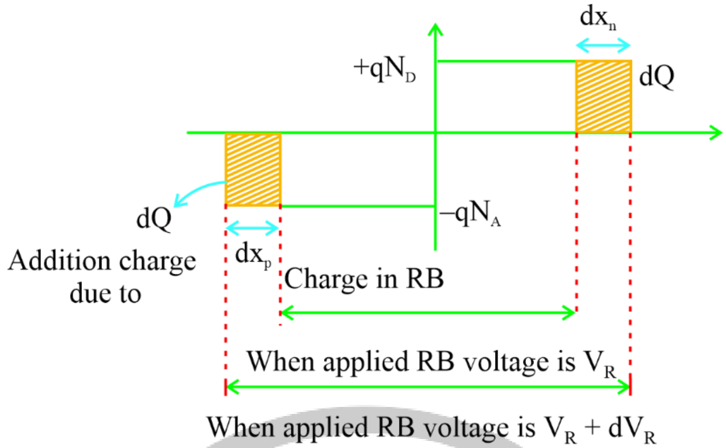
$$E = \frac{-qN_A}{\varepsilon}[x + x_P]; -x_p \le x \le 0$$

$$E = \frac{-qN_D}{\varepsilon}[x_n - x]; 0 \le x \le x_n$$

$$E_{max} = \frac{-2(V_{bi}+V_R)}{W}$$

4.3. Junction Capacitance

We have a separation of +ve & –ve changes in the depletion reason therefore a capacitance is associated with p – N junction, this capacitance is called as junction capacitance or depletion layer capacitance



$$C = qN_DA\sqrt{\frac{\varepsilon}{2q},\frac{N_A}{N_D}\times\frac{1}{N_A+N_D}\times\frac{1}{(V_{bi}+V_R)}}$$

$$C \propto \frac{1}{\sqrt{V_{bi}+V_R}}$$

$$\frac{C}{A} = C' = \sqrt{\frac{\varepsilon q}{2}\frac{N_AN_D}{N_A+N_D}\times\frac{1}{V_{bi}+V_R}} \quad \text{(Capacitance per unit area)}$$

$$C' = \frac{E}{W}\ V/cm^2 \ \& \ C = \frac{AE}{W}\ F$$

> **Note :** Where $V_R = 0 \Rightarrow C = C_0 \longrightarrow$ max depletion capacitance
>
> $$\frac{C}{C_0} = \sqrt{\frac{1}{1+V_R/V_{bi}}}$$

Under revers bias the current due to majority is low

- It is blocking the flow of majority carrier in R.B, so, the crossing of junction become block, hence reverse bias is also called blocking bias
- Under RB only minority carries will be falling from the barrier potential and they contribution majority carrier current (I_0)

I_0 = thermally generated or minority carrier current or reverse saturation current or leakage current

I_0 = μ A(for Ge)

I_0 = nA(For Si diode)

Highly sensitive to temp (I_0 inverse with temp. increase)

I_0 is independent of the applied reverse bias voltage that is I_0 is saturated w.r.t applied V_{RB} and hence called saturation current

I_0 is reverse current flow from n to p.

As temp increase minority carrier are generated

For 1°C increase in temp = I_0 increase by 7%

I_0 is a drift current because thus current is due to the field intensity, which is passing through junction

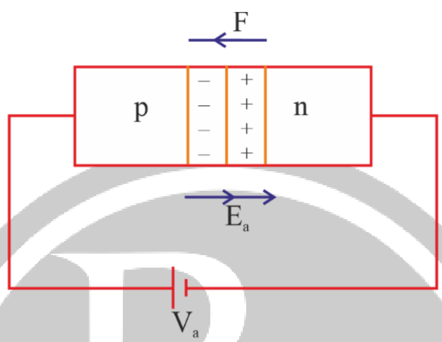
$$E_{Peak} = \frac{-V_j}{w/2} = \frac{-2V_j}{w}$$

$$E_{Peak} = \frac{2\left[V_0 + |V_{RB}|\right]}{W}$$

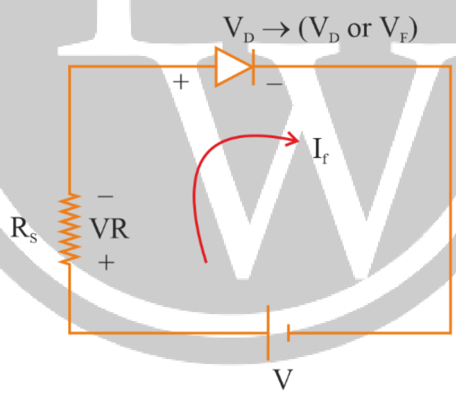
$$W = \frac{\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)|E_{peak}| \text{ depletion width in terms of } E_{Peak}$$

Forward Bias (FB)

When a positive potential is applied on p – side w.r.t *n* – side then applied bias is called as forward bias



When any type of p – n junction is forward biased limiting resistance must be connected in series with the diode, the limiting resistance and diode working as potential divider network



Forward voltage, across the diode is V_D

$$V_D \leq 0.5 \text{ V for Ge}$$

$$V_D \leq 0.9 \text{ V for Si}$$

$$V = V_R + V_D$$

$$V = I_f R_s + I_f R_f$$

Where, I_f = diode current/forward bias current

The majority carriers of P & n regions will be moving towards the junction and neutralize the immobile ions so that the region of immobile charges gets reduced that is width of the depletion layer is reduced

E_s and E_v are in opposite direction

Experimentally found resultant is directed from *n* to *p*.

The potential barrier is reduced by $|V_d|$ under forward bias

$$V_j = V_0 - |V_D|$$

Case I :

$V_D < V_0$, the diode is in forward biased and non conducting state and its is "Off state" or "zero state"

Case II :

$V_D = V_0$, effect of Barriers is "Nullified "

Case III:

More majority carriers will be crossing the junction and the junction and the forward current is large and the forward current will be exponentially increasing with V_d.

Excess Majority Carrier in Both Side

In normal equilibrium

$$n_{p_0} = n_{n_0} e^{-\frac{V_{bi}}{V_T}} \qquad p_n = p_{p_0} e^{-V_{bi}/V_T}$$

Where, $n_{n_0} \rightarrow$ e^- concentration on n – side (majority carrier)

$n_{p_0} \rightarrow$ e^- concentration of p – side (minority carrier)

After application of forward bias, as due to barrier potential

$$n_p = n_{p_0} e^{V_0/V_T} \quad p_n = P_{n_0} e^{-V_0/V_T}$$

Where, n_p = e^- concentration at the edge of depletion region on p – side

And p_n = hole concentration at the edge of depletion region on n – side

Forward Bias Current

$$I_f = \text{Diffusion current (P to n)}$$

$$I_f = I_0\left[e^{V_d/\eta V_T} - 1\right]$$

Where, V_d = voltage across diode (p to n) forward bias)

N = utility or ideality factor

V_T = thermal voltage ; KT/q

η = 1 = for large currents, eq : Ge

η = 2 = for small current , eq : Si

Default value of η = 1

$$I_0 = \text{Reverse saturation current (Drift current)}$$

$$I_0 = \left[\frac{AqD_p n_i^2}{L_P N_D} + \frac{AqD_n n_i^2}{L_n N_A}\right]$$

$$I_F = I_{diff} = \frac{AqD_p n_{i^2}}{L_P N_P}\left(e^{\frac{V_d}{\eta V_T}} - 1\right) + \frac{AqD_n n_i^2}{L_n N_A}\left(e^{\frac{V_d}{\eta V_T}} - 1\right)$$

$$I_{diff} = I_{p\,diff} + I_{n\,Diff}$$

$$I_{diff} = \frac{AqD_p n_i^2}{L_p N_D}\left(e^{V_d/\eta V_T} - 1\right) + \frac{qD_n n_i^2}{L_n N_A}\left(e^{V_d/\eta V_T} - 1\right)$$

Forward current is always independent of temperature because this current is carried by majority carrier & minority carrier concentration is always independent of temperature.

$$I_F = I_0\left[e^{V_d/\eta V_T} - 1\right]$$

$$V_d = \text{forward bias across p – n junction}$$

$$0 \le V_d \le V_{bi}$$

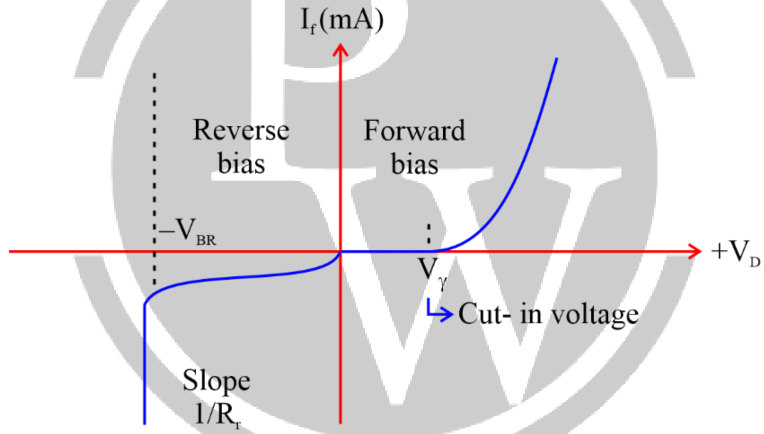
$$w \propto \sqrt{V_{bi} - V_a}$$

For $V_{bi} > V_a$, w will comes to be imaginary which is not possible

$$V_D = \eta V_T \ell n\left(\frac{I_f}{I_0}\right)$$

$$\frac{dV_d}{dt} = -2.5\,mV/°C$$

VI Characteristics of p – n junction diode :



When p – n junction is reverse biased the reverse voltage must be always less than breakdown voltage of the device otherwise the diode will be destroyer

$$\text{Breakdown voltage} = V_{BR} \text{ or } B_V$$

$$V_{BR} \propto \frac{1}{\text{Doping concentration}}$$

$$V_{BR} = \frac{\varepsilon E^2}{2q(\text{Doping concentration})}$$

Cut in Voltage (V_γ) :

- Also called offset voltage (in FET's) or called threshold voltage (in tubes)
- Min voltage required so that the forward current just passes into diode

$$V_\gamma = 0.1 \text{ v to } 0.5 \text{ v [typical = 0.2]}$$

$$\min V_\gamma = 0.1\text{v or } 100 \text{ mv}$$

cut in voltage decrease with increase in temperature

v_y reduced by 2.5 volt for 1° c increase in temperature

4.4. Small Signal Equivalent Circuit of Diode

Diode Resistance

In reverse biased : Ideally current is zero then R = ∞ , open circuit practically I = I_0 , R is very large

In forward biased

$$I_F = I_0\left[e^{\frac{V_d}{\eta V_T}-1}\right]$$

$$\frac{dI_F}{dV_d} = \frac{I_F}{\eta VT} \quad \text{admittance of diode (g)}$$

$$\frac{l}{g} = r_f = \frac{\eta V_T}{I_F} \quad \text{forward resistance or dynamic resistance}$$

Diffusion Capacitance (C_D)

C_D = Rate of change of injected minority charges w.r.t changes in forward voltage

C_D is due to a change in injected minority charge

C_D is the junction capacitance in a forward biased

$$C_D = C_j = A\varepsilon/W$$

$$C_D \propto A$$

$$C_D \propto 1/W$$

$$C_D \propto \sqrt{\text{Doping concentration}}$$

$$C_D = \tau \cdot g$$

Where g = dynamic conductance or reciprocal of dynamic resistance

If g = $1/r_f$ = I_f / ηVT

Then, $C_D = \dfrac{\tau}{r_f}$ $\qquad C_D = \dfrac{\tau . I_f}{\eta v_T}$ forward $C_D \propto I_f$

Transition capacitance (C_T)

$$C_T = C_J = \frac{A}{\sqrt{\frac{2}{q\varepsilon}\left(\frac{N_A + N_D}{N_A N_D}\right)V_O\left(1+\left|\frac{V_{RB}}{V_0}\right|\right)}}$$

$$C_T = C_J = \frac{A\sqrt{\frac{q\varepsilon N_A N_D}{2V_0[N_A + N_D]}}}{\sqrt{1+\left|\frac{V_{RB}}{V_0}\right|}}$$

❐❐❐

5 SPECIAL DIODES

5.1. Varactor Diode

As the larger variations, in the diode capacitance. The varactor diode is always operates under reverse bias conditions. It is variable capacitance diode with linearly doped P and N regions. It is voltage variable capacitance.

$$C_T = \frac{C_{T_0}}{\left(1+\frac{V_{RB}}{V_{bi}}\right)^{1/n}}$$

n = 2 for step graded Junction

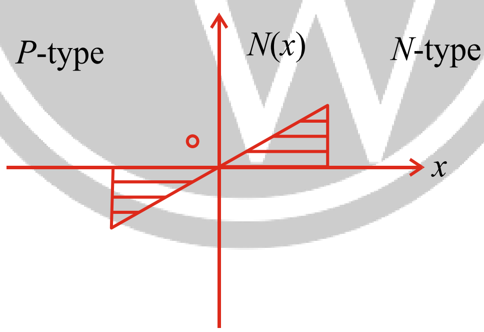
n = 3 for lineally graded Junction.

In linearly graded junction the junction the doping profile is defined as :

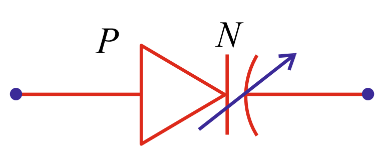
$$\boxed{N_{(x)} = N_0 x}$$

For P region : $N_a(x) = N_{ao}x$

For N region : $N_d(x) = N_{do}x$



Symbol:



New for varactor diode : $\boxed{C_T = \frac{C_{T_0}}{\left(1+\frac{V_{RB}}{V_{bi}}\right)^{1/3}}}$

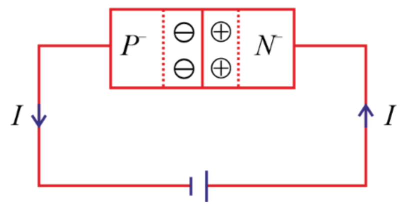
It is use in voltage-controlled oscillators (VCO), Radio frequency fitters and frequency and phase modulators.

It is also use in automatic frequency control devices self-balancing of AC bridges.

5.2. Photo Diode

It converts light energy into electrical energy. Photo diode has lightly doped P and N region, so the depletion region will have slightly larger depletion width (W), The advantage of larger W is, it will absorb larger number of photons from the light energy near the junction. So that both side by minority will be created near the junction.

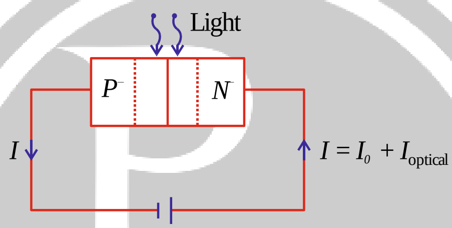
The falling photons will break the co-valent bonds and create minority carious of both side. Impact on the reverse bias current hence photo diode is always operates under reverse bias.



To absorbed more photons, photo sensitive material ZnS or CaS is coated over the depletion region.

In reverse bias :

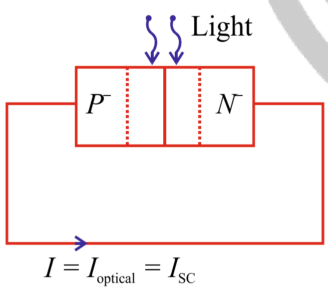
$$I = I_0, \text{ when no light falls.}$$

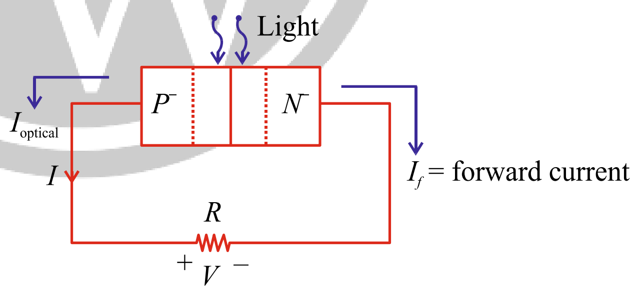


$I_{optical} \rightarrow$ Current due to excess carriers generated due to optical energy. (Diffusion current)

Short Circuit Current:

As there is no reverse voltage ($I_0 = 0$)





V = IR, The voltage V start bias the PN junction as forward bias, hence current I :

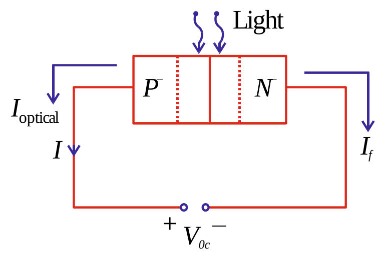
$$I = I_{optical} - I_f$$

$$\boxed{I = I_{optical} - I_o\left[e^{V/nV_T} - 1\right]}$$

Open Circuit Voltage:

$$I = I_{optical} - I_f = 0$$

$$\boxed{V = V_{oc}}$$

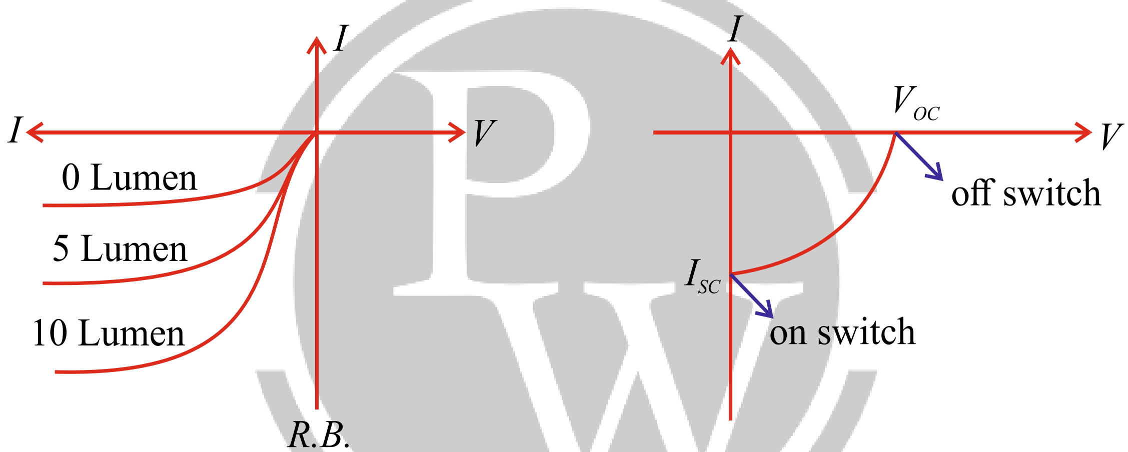


$$I_{optical} - I_0\left[e^{V_{oc}/\eta V_T} - 1\right] = 0$$

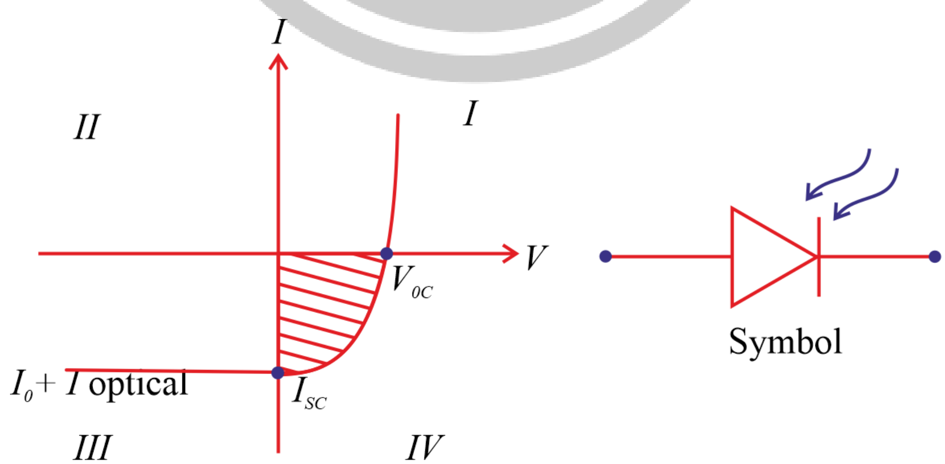
$$V_{oc} = \eta V_T \ell n\left[\frac{I_{optical}}{I_o} + 1\right]$$

$$V_{oc} = \eta V_T \ell n\left[\frac{I_{sc}}{I_o} + 1\right]$$

Characteristics :



It is a light operated switch with switching time is in μ seconds, and it is almost 1000 times faster than the normal diode.



As it converts optical energy into electrical energy, it is widely use in satellite communication as a transformer.
The only disadvantage of photo diode is, it has smaller power handing capacity. lubrication of PIN photo diode, which has larger power handling capacity.

Quantum Efficiency : [Q_e]

$$Q_e = \frac{\text{No. of electrons collected}}{\text{No. of incident photons}} = \frac{r_e}{r_p}$$

$$Q_e = \frac{I_{\text{optical}} \times \dfrac{hv}{q}}{P_0} \times 100\%$$

P_o = incident power.

$$\boxed{Q_e = R.\frac{hv}{q}}$$

Responsivity : [R]

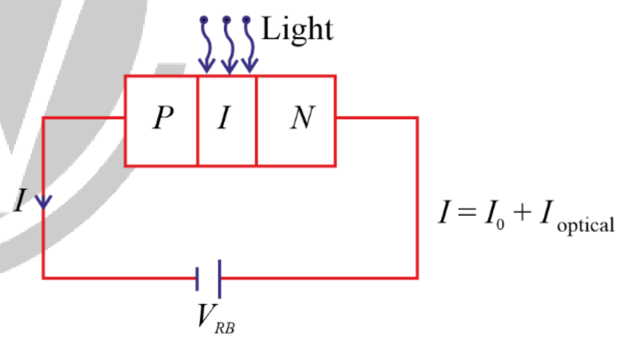
$$R = \frac{\text{output current}}{\text{incident power}} = \frac{\text{optical current}}{\text{Incident power}}$$

$$\boxed{R = \frac{I_P}{P_o} = \frac{I_{optical}}{P_o}} \; A/watt$$

$$\boxed{R = \frac{Q_e}{\dfrac{hv}{q}} = \frac{qQ_e}{hv} = \frac{qQ_e\lambda}{hc}}$$

3. PIN Photo Diode :

PIN diode has intrinsic region sandwiched between P and N region. Which offers high resistivity and provide larger power handling capacity.

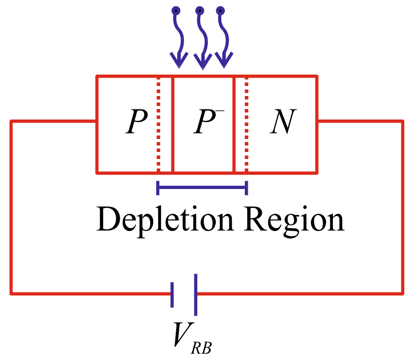


Because of intrinsic region ideal PIN Diode does not have any PN Junction.

To create PN Junction 'I" region is replaced by lightly doped P region. Which is called as π–region or I-region is replaced by lightly doped N-region. Which is called V-region.

In this overall π region is swap out and covered by depletion region.

$$\boxed{V_{RB} = V_{swap\ out}}$$



PVN Photon Diode :

In this overall v-region is swap out and covered by depletion region.

$$\boxed{V_{RB} = V_{swap\ out}}$$

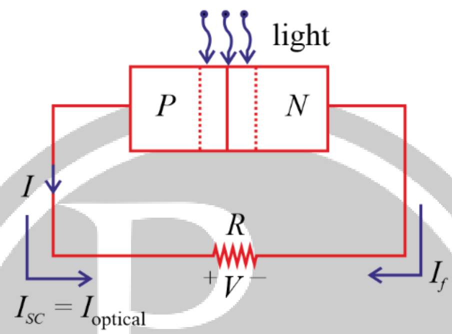
Both PπN and PγN diodes operate after swapping out of π and γ region in order to get larger current.

PIN diode is as faster switch than the photo diode and the switching time is in nS (nano seconds)

Due to larger power handling capacity PIN diode is used in microwave applications.

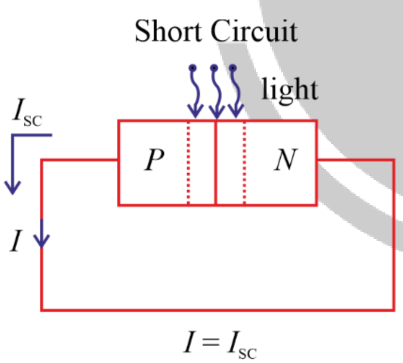
4. Solar Cell :

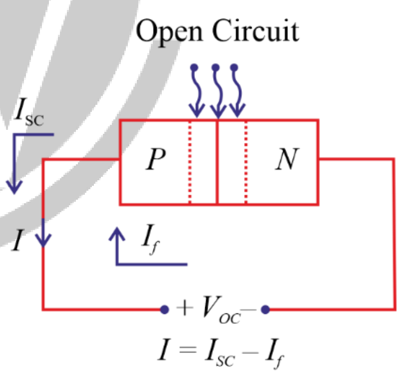
The working principle of solar cell is similar to the photo diodes.
Consider a PN Junction with resistive load.



This drop v will bias PN Junction, in forward bias.

$$\boxed{I = I_{\text{optical}} - I_f}$$





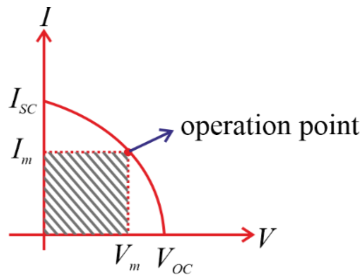
$I = I_{sc} - I_f$

$$V_{oc} = \eta V_T \ell n\left[\frac{I_{optical}}{I_O} + 1\right]$$

$$V_{oc} = \eta V_T \ell n\left[\frac{I_{sc}}{I_O} + 1\right]$$

$$\boxed{V_{oc_1} - V_{oc_2} = \eta V_T \ell n\left(\frac{I_{sc_1}}{I_{sc_2}}\right) = \eta V_T \ell n\left(\frac{J_{sc_1}}{J_{sc_2}}\right)}$$

Characteristics :



Maximum power delivered (p)

$$\boxed{P = I.V}$$

$$P = \left[I_{\text{optical}} - I_o\left(e^{V/\eta V_T} - 1\right)\right] \times V$$

$$\text{For } \frac{dP}{dV} = 0$$

At this, the value of V will give maximum power. That value of V and corresponding value of I is known as operating point, i.e. V_m and I_m.

$$\boxed{P_{\text{max}} = I_m . V_m}$$

Responsivity, $$\boxed{R = \frac{I_{optical}}{P_{in}}} \ A/watt.$$

Conversion efficiency : [η]

$$\eta = \frac{\text{Electrically genrated power}}{\text{Incidert optical power}}$$

$$\boxed{\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{I_m V_m}{P_{in}}}$$

$$\boxed{V_m = \frac{hv}{q}}$$

$$\boxed{\eta = \frac{I_{optical} \times hv}{P_{in} \times q} = R.\frac{hc}{q\lambda}}$$

$$\boxed{\eta = \frac{1.24\,R}{\lambda(in\ \mu m)}}$$

Fill factor : [FF]

It is the ratio of operating power and the maximum theoretical power.

$$\boxed{FF = \frac{I_m V_m}{I_{sc} V_{oc}}}$$

5. LED (Light Emitting Diode) :

LED works on the principle of electro luminescence. It is the property by which light energy comes out due to electron hole recombination.

It always operates under forward bias, so that large recombination happen at the junction and produce light.

Light Intensity [I] ∝ I_f. (forward current).

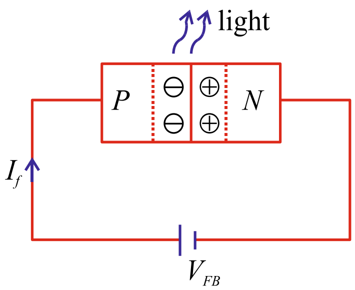
LEDs are fabricated by direct Band Gap semiconductors.

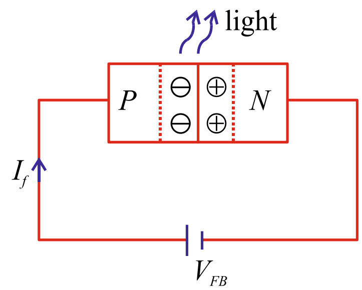
GaAs → Infrared light

GaA → Blue light

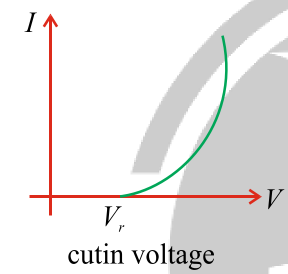
GaAsP → Red or yellow light

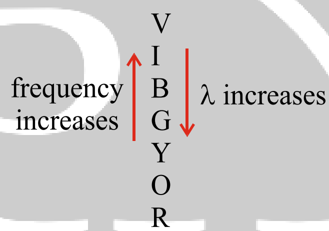
GaP → Red or Green





Characteristics:





$$\lambda = \frac{1.24}{E_g(ev)} \mu m.$$

$$\lambda_{max} = \lambda_{red}, \quad \lambda_{min} = \lambda_{violet}$$

$\lambda_R > \lambda_0 > \lambda_Y > \lambda_G > \lambda_B > \lambda_I > \lambda_V$

$E_{gR} < E_{g0} < E_{gY} < E_{gG} < E_{gB} < E_{gI} < E_{gV}$

$V_{biR} < V_{biO} < V_{biY} < V_{biG} < V_{biB} < V_{biI} < V_{biV}$

Also $V_r \propto V_{bi}$ Built in voltage

V_r = Cutin voltage

V_{bi} = Built in voltage

Internal Efficiency : [η_{int}]

$$\eta_{int} = \frac{\tau_r}{\tau}; \quad \frac{1}{\tau} = \frac{1}{\tau_r} + \frac{1}{\tau_{nr}}$$

τ = total recombination carrier lifetime

τ_r = Radiative recombination carrier lifetime.

τ_{nr} = Non-radiative recombination carrier lifetime.

Internal Power : [P_{int}]

$$P_{int} = \eta_{int} \cdot \frac{hCI}{\lambda q} \text{ watt}$$

Emitting Power : [P_e]

$$Pe = \frac{P_{\text{int}}.F\eta^2}{4\eta_x^2}$$

$F \rightarrow$ Transmission factor between LED material and medium.
$\eta \rightarrow$ Refractive index of the medium.
$\eta_x \rightarrow$ Refractive index of the material.

External power Efficiency : η_{ep}

$$\eta_{ep} = \frac{Pe}{P} \times 100\%$$

P = input Power.

Power conversion or coupling power efficiency : [η_{cp}]

$$\eta_{cp} = \frac{P_c}{P} \times 100\%$$

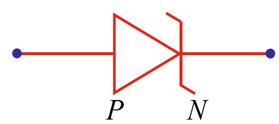
$$\boxed{\eta_{cp} = \frac{P_c}{IV} \times 100\%}$$

Zener Diode :

It is slightly highly doped diode, specially designed to operate under breakdown region.

Breakdown is a phenomena in which, large number of covalent bonds will be broken and this will change the minority carrier concentration significantly. Hence breakdown occurs in reverse bias. In forward bias only majority carriers will present and due to this breakdown is not possible in forward bias.

Symbol



Breakdown are of two types:

1. Zener breakdown
2. Avalanche breakdown

Zener Breakdown

In Zener breakdown both P and N region are highly doped, due to that barrier energy will be large and depletion width will be smaller and when we applied reverse bias voltage, the $\vec{E}$ -field in the depletion region will be increasing and at reverse bias voltage equals to the breakdown voltage, the electric field will become very large and called as critical $\vec{E}$ -field $\left(\vec{E}_{crit}\right)$ dut to that covalent bonds at the junction will be broken and current abruptly increases. It is negative temperature coefficient

- Zener breakdown is due to longer(E) field intensity in the depletion region
- Zener breakdown occurs at low voltages.
- When temp will increase covalent bonds will be broken current will start increasing due to that the breakdown occurs at low voltages.

$$\frac{dv_z}{dt} = \ominus ve \rightarrow \ \ominus\text{ve temp. coefficient}$$

This indicates Zener breakdown is $\ominus$ve temp. coefficient

5.3. Avalanche Breakdown

Avalanche lockdown occurs in lightly doped diode due to that the barrier is very small and depletion width will be larger due that $e^{\ominus}$ will spend more time when move for p region $\rightarrow n^-$ region and due to larger K.E. e^- will be strike on the covalent bond will be broken and one e$^{\ominus}$ will be generated again the unmuted e$^{\ominus}$ will impact on the another covalent bond and further e$^{\ominus}$ will be generated. After impact the e$^{\ominus}$ will be migrated into the *n*-region.

Breaking of covalent bond due to impact energy in called as impact ionization which gives e$^{\ominus}$ multiplication

$$T\uparrow \rightarrow \mu\downarrow \rightarrow V_d\downarrow \rightarrow \frac{1}{2}mV_d^2\downarrow$$

$$\Downarrow$$

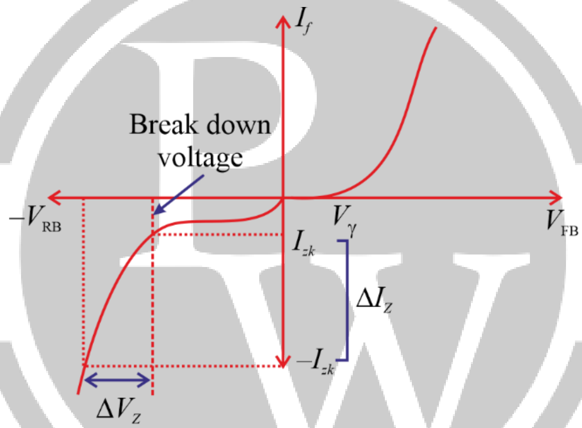
$$\text{For } qVRB\uparrow \rightarrow \frac{1}{2}mV_d^2\uparrow$$

when temp will increase mobility will decrease due to lattice scattering which make V_d smaller and the K.E. of e$^{\ominus}$ will be small and for breakdown of the diode equal high R.B voltage when temp (↑) breakdown voltage in avalanche breakdown(↑)

$$\frac{dV_z}{dt} = \oplus ve$$

This indicates ⊕ve temp coefficient of avalanche breakdown.

Characteristics : (Zener Diode)



Dynamic resistance, $r_z = \frac{\Delta V_z\uparrow}{\Delta I_z\uparrow}$ = dynamic resistance of Zener diode.

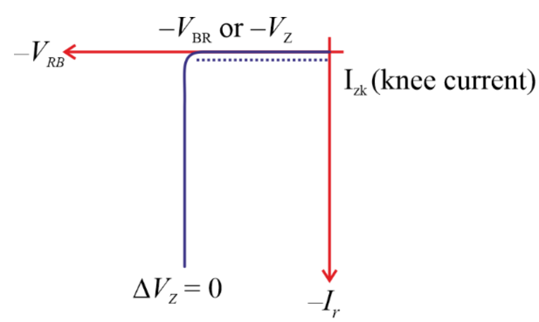
V_γ = 0.7 V (Zener Diode is always laid of Si)

$r_z \rightarrow$ very small (1Ω – 10Ω)

The min current required for a Zener diode to be operate in R.B. Region is known current

$\because \quad r_z = \frac{\Delta V_z}{\Delta I_z} = 0$

$\Rightarrow \quad r_z = 0$



If $V_{RB} < V_z$

⇓

Normal diode in RB

If $V_{RB} > V_z \Rightarrow$ Zener diode in Breakdown region (conducting)

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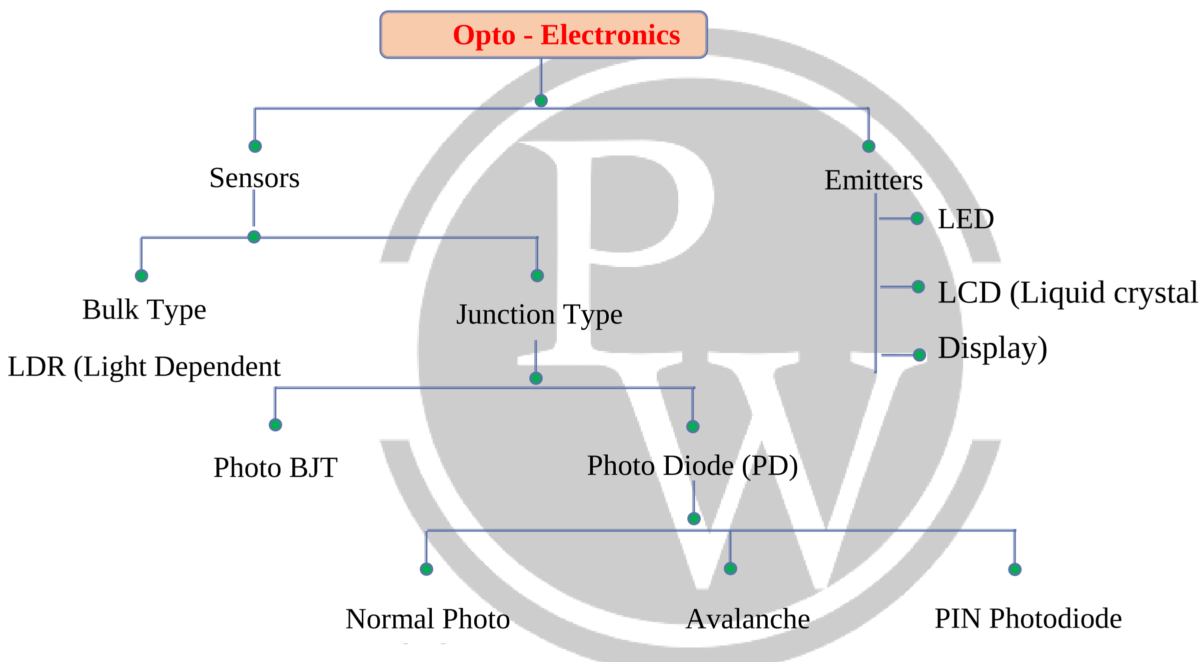
6 OPTO-ELECTRONICS AND QUASI FERMI LEVELS

6.1. Opto-Electronics and Quasi Fermi Levels



When Light falls at

Junction type of sensors or bulk type of sensors then due to absorption of photon. The Covalent bonds will be broken and Electron – Hole pairs will generate. Multiple photons will generate multiple EHP's

To generate EHP

$$\text{Photon energy} = h\nu$$

h = planks constant = 6.62×10^{-34} J – sec.

ν = frequency (Hz)

$$\nu = \frac{c(\text{Speed of light})}{\lambda(\text{wave length})}\text{Hz.}$$

$hv \geq E_g$ (energy band gap)

$$\frac{hc}{\lambda} \geq E_g$$

$$\lambda \leq \frac{hc}{E_g}$$

$$h = \frac{6.62\times10^{-34}}{q} \text{ ev-sec.} = \frac{6.62\times10^{-3}}{1.6\times10^{-19}} \text{ ev - sec}$$

$c = 3 \times 10^8$ m/sec.

$$\lambda \leq \frac{1.24}{E_g(ev)} \mu\text{m}$$

Critical wave length $\lambda_c = \dfrac{1.24}{E_g(ev)} \mu m$

Generation rate (G_L) due to irradiation of light :

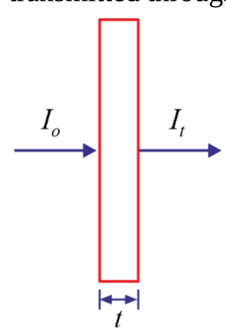
$$G_L = \frac{\text{Excess minority carrier concentration}}{\text{Minority carrier life time}}$$

When light falls equal number of e^- and holes will be created

Beer-Lambert Law

This states that, if light passes through the sample then some part of light will get absorbed and rest will be transmitted through the sample. This transmitted part of light depends on the absorption coefficient (α).

$$I_t = I_o e^{-\alpha t}$$



$I_t \rightarrow$ Transmitted Intensity

$I_o \rightarrow$ Incident Intensity

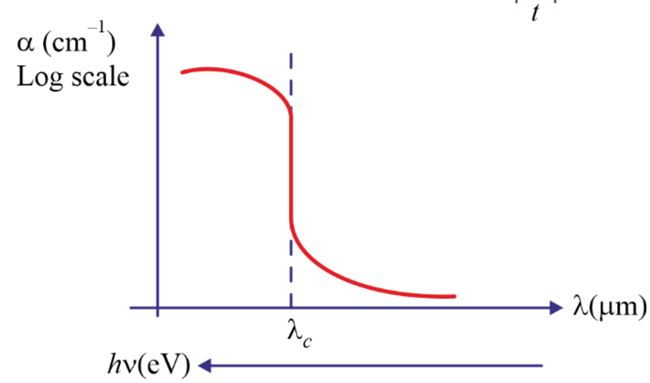
$\alpha \rightarrow$ Absorption coefficient (cm^{-1})

$t \rightarrow$ thickness of the sample

Absorbed Intensity = $I_o - I_t$

Absorption coefficient (α), depends on the material and associated wavelength (λ) of light.

$$\lambda_c = \frac{1.24}{E_g(eV)} \mu m$$



Let *n* – type SC :

Before illumination : $n_{no} = N_D$

$$p_{n_0} = \frac{n_i^2}{n_{n_0}} = \frac{n_i^2}{N_D}$$

After illumination :

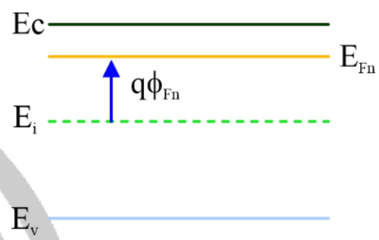
$$n_n = n_{n_0} + \Delta n_n$$
$$p_n = p_{n_0} + \Delta p_n$$
$$\Delta n_n = \Delta p_n$$

$\Delta n_n \rightarrow$ Excess e^- concentration

$\Delta P_n \rightarrow$ Excess hole concentration

$$G_L = \frac{\Delta n_n}{\tau_{P_0}} = \frac{\Delta P_n}{\tau_{P_0}} \ \text{m}^3/\text{sec or cm}^{-3}\ \text{s}^{-1}$$

Before Illumination:



$\Phi_{fn} \rightarrow$ Fermi potential for electrons

$$\phi_{fn} = \frac{KT}{q}\ell n\left(\frac{n_{no}}{n_i}\right) = \frac{KT}{q}\ell n\left(\frac{N_D}{n_i}\right)$$

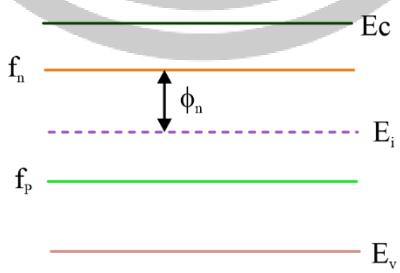
$$q\phi_{fn} = KT\ell n\left(\frac{N_D}{n_i}\right)eV$$

f_n = Quasi fermi level of e^-

f_P = Quasi fermi level of hole

When we starts illuminating light over the semiconductor (n – type), due to EHP generation. There will be significant change in hole concentration and almost insignificant change in e^- concentration. Due to that that there will be change in Quasi fermi level of holes (f_p) and almost no change in quasi fermi levels of e^- (f_n)

After illumination :



More illumination gives more shift in F_P

$$f_n - E_i = KT\ell n\left(\frac{n_n}{n_i}\right)eV$$

$$E_i - f_p = KT\ell n\left(\frac{P_n}{n_i}\right)eV$$

f_n and ϕ_{fn} is consider to be negative as it goes upwards than E_i(Fermi level of intrinsic) and f_p and ϕ_{FP} is consider to be positive as it goes down wards than E_i.

Similarly for P – type SC:

Before illumination :

$$p_{p0} = N_A$$

$$n_{p_0} = \frac{n_1^2}{p_{p_0}} = \frac{n_i^2}{N_A}$$

After illumination :

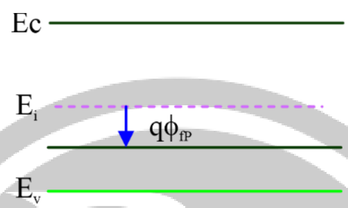
$$p_p = p_{p0} + \Delta p_p$$

$$n_P = n_{p0} + \Delta n_p$$

$$= n_p = \Delta p_p$$

$$G_L = \frac{\Delta n_p}{\tau_{no}} = \frac{\Delta P_p}{\tau_{no}} \text{ cm}^{-3}\text{s}^{-}1$$

Before Illumination :



$\Phi_{fP} \rightarrow$ fermi potential for holes

$$\phi_{f_P} = \frac{KT}{q}\ell n\left(\frac{P_{PO}}{n_i}\right) = \frac{KT}{q}\ell n\left(\frac{N_A}{n_i}\right)$$

$$q\phi_{f_P} = KT \ln\left(\frac{N_A}{n_i}\right) eV$$

Here due to EHP generation the change in e^- concentration will be significant and change in hole concentration will be insignificant. Hence change in f_n will be significant and f_P will be insignificant

After illumination:

More illumination gives more shift in f_n.

$$f_n - E_i = KT\ell n\left(\frac{n_P}{n_i}\right) eV$$

$$E_i - f_P = KT\ell n\left(\frac{p_P}{n_i}\right) eV$$

Conductivity due to illumination:

$$\sigma_{opt} = \Delta n q \mu_n + \Delta P q \mu_p \text{ ℧/cm}$$

Where, Δn = change in e^- concentration

$\Delta P \rightarrow$ change in hole concentration

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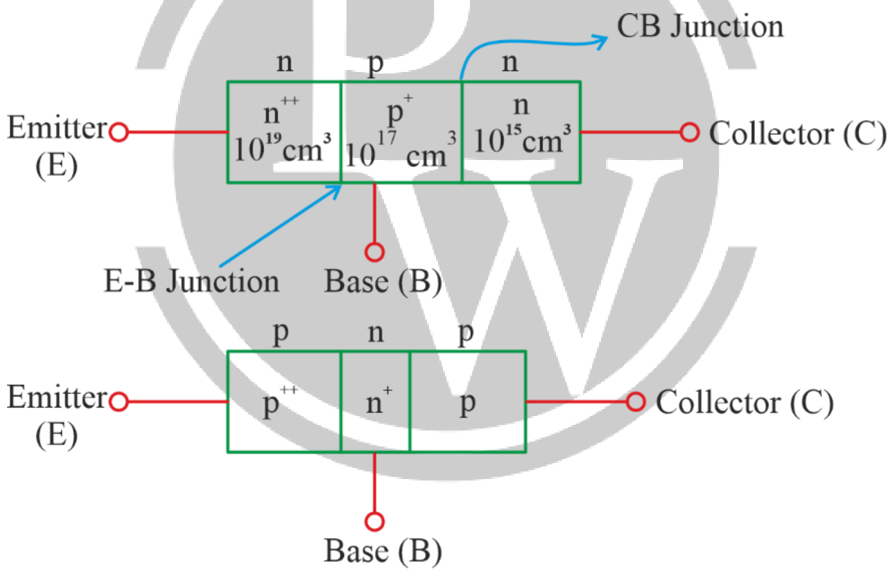
7 BIPOLAR JUNCTION TRANSISTOR

7.1. BJT (Bipolar Junction Transistor)

- Transistor is a multijunction semiconductor device that together with other circuit element is capable of current gain, voltage gain and signal power gain, therefore it is an active device whereas diode is passive device.
- The basic transition action is the control of current at one terminal by the voltage applied across other two terminal of the device.

7.1.1. Basic Structure of BJT



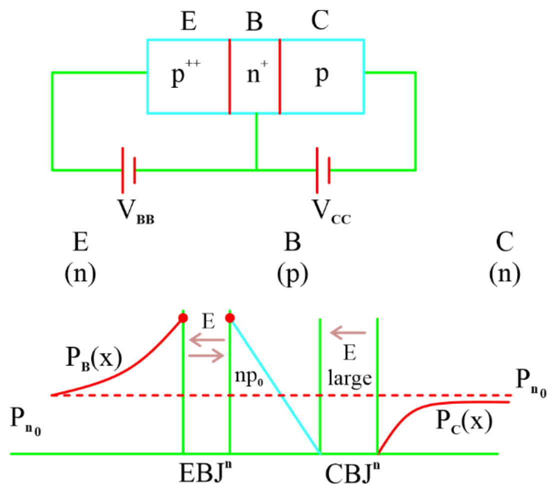
- BJT has 3 separately doped region and 2 p-n Junction, 3-terminal connection are emitter, base and collector.
- The width of the base region is small as compared to the minority carrier diffusion length.
- The emitter region has the largest doping concentration region and base region has the smallest.
- Bipolar Junction transistor is not a symmetrical device.

7.1.2. Basic Operation of BJT

- Forward active mode

  Where, EB Junction is forward Bias

  And CB junction is in reverse Bias



- Distribution of minority carriers in npn transistor in forward active mode.
- The BE junction is forward biased and CB junction is reverse biased. This configuration is called the forward active operating mode.
- The electron from the emitter are injected across the base-emitter junction into the base. These injected electrons create an excess concentration of minority carrier in base.
- Similarly holes from the base injected across the base-emitter junction into the emitter.
- These injected electrons and holes create an excess concentration of minority carrier in the base and emitter respectively.
- The base collector junction is reverse biased so the minority carrier electron concentration at the edge of base collector voltage and the two close enough junction are said to be interacting p-n junction.

7.3. Simplified Current Relation in BJT

(1) Collector Current:

- Assuming ideal linear electron distribution in base, then collector current can be written as diffusion current.

$$I_c = qDn\frac{dn}{dx}\cdot A_{BE}$$

$$I_c = I_s \cdot e^{V_{BE}/V_T}$$

where, $$I_s = \frac{qD_n A_{BE} n_{BO}}{x_B}$$

$A_{BE} \rightarrow$ Base emitter junction Area

$N_{BO} \rightarrow$ Thermal equilibrium electron concentration in base region

$x_B \rightarrow$ Neutral base width (not considering space charge region)

(2) Emitter Current:

- I_{E_1} = It is due to the flow of electron injected from emitter to base, thus ideally it is equal to collector current.
- I_{E_2} = Base – Emitter junction is forward based majority carrier holes of base injected across the base emitter junction into the emitter.

$$I_{E_2} = I_{S_2} \cdot e^{V_{BE}/V_T}$$

Where $I_{S_2} \rightarrow$ it includes minority carrier hole parameters in emitter region.

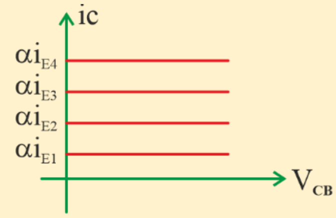
- Now, $$I_E = I_{E_1} + I_{E_2}$$
$$I_E = \left(I_S + I_{S_2}\right)e^{V_{BE}/V_T}$$

$\frac{I_C}{I_E} = \alpha \rightarrow$ Common-Base current gain factor

$I_C = \alpha I_E$ as, $I_E > I_C$ so $\alpha < 1$

Note:

- Since I_{E_2} is not a part of the basic transistor action we would like to be this component as small as possible in order to make common base current gain close to unity.
- Ideally I_C is independent of V_{CB} as long as collector base junction is reverse bias so we can say BJT act as constant current source
- Ideal BJT I-V characteristics in common base configuration.



(3) Base Current:

- The emitter current I_{E_2} is a base emitter junction current so that this current is also a component of base current.
- Since majority carrier holes in the base are disappearing, they must by resupplied by a flow of positive charge into the base terminal, this flow of charge is I_{Bb}.
- The total base current is the sum of I_{Ba} and I_{Bb}.

$$I_B = I_{Ba} + I_{Bb}$$

- The ratio of i_c and i_b is also a constant

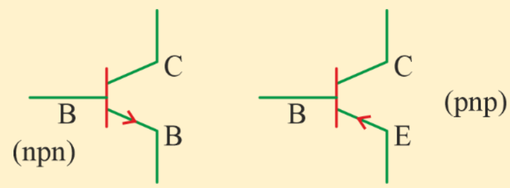
$$\frac{I_C}{I_B} = \beta \Rightarrow I_C = \beta I_B$$

Where, β = common-emitter current gain factor.

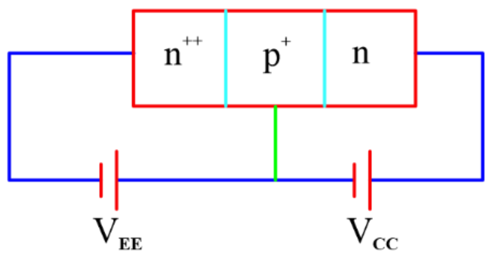
Note: Applying kCL

$$I_E = I_C + I_B$$

- $\frac{I_C}{I_B} = \beta \Rightarrow I_C = \beta I_B$

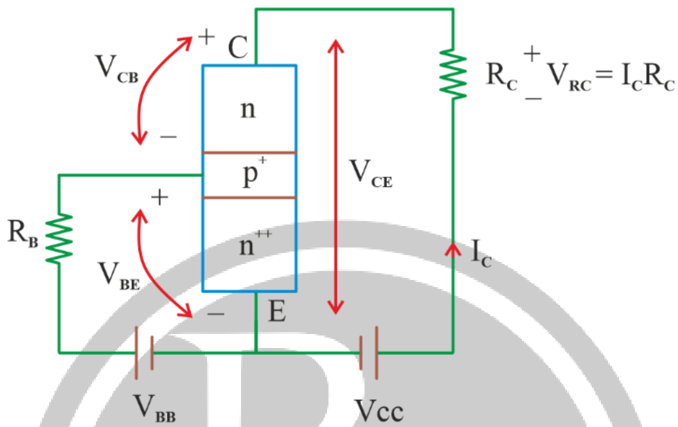


7.3.1. Other Operating Models of BJT



BE Junction	CB Junction
FB	RB $\rightarrow$ Forward active mode
RB	RB $\rightarrow$ Cut-off mode
FB	FB $\rightarrow$ Saturation mode
RB	FB $\rightarrow$ Inverse Active mode

Common Emitter Configuration:



If $V_{CB} > 0$, then Reverse Bias

IF $V_{BE} > 0$, then Forward Bias

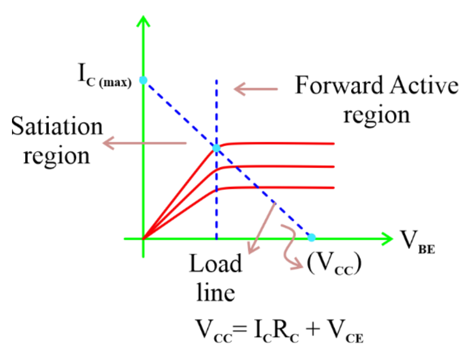
$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CC} = V_{CE} + V_{RC}$$

$$V_{CE} = V_{CB} + V_{BE}$$

If $V_{BE} \uparrow$es $\rightarrow I_C\uparrow \rightarrow V_{RC}\uparrow \rightarrow V_{CE}\downarrow \rightarrow V_{CB} \downarrow$es

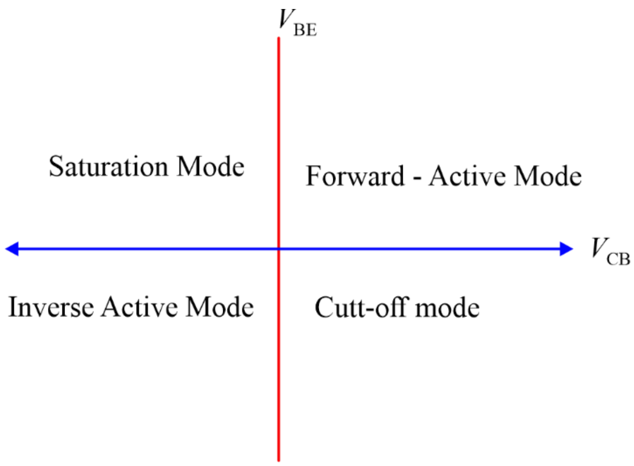
- If V_{CC} is large enough and V_{RC} is small enough the $V_{CB} > 0$ therefore base collector junction is RB and BE junction is FB already, this condition is of forward active region of operation.
- At a certain point of V_{BE}, I_C become large enough to make $V_{CB} = 0$, Beyond this point if I_C is slightly increased the V_{CB} become negative and CB junction becomes FB and IC is no longer controlled by BE voltage i.e., the relation $I_C = \beta I_B$ will no longer hold.
- O/P characteristics



$$V_{CC} = I_C R_C + V_{CE}$$

Work as an amplifier or current source

For npn:



Expression for 'β': (Current gain factor)

$$\beta = \left[\frac{D_P}{D_n} \cdot \frac{N_B}{N_E} \cdot \frac{x_B}{L_P} + \frac{x_B^2}{2\tau_{no} p_n}\right]^{-1}$$

Here x_B is very small and $N_E \gg N_B$

- The current gain factor β, depends on two factors
  (i) Effective Base width (x_B)
  (ii) Ratio of doping concentration in Base and Emitter Region (N_B/N_E)
- Prismatic and non-prismatic

Relation between α and β:

$$\alpha = \frac{\beta}{\beta+1} \text{ and } \beta = \frac{\alpha}{1-\alpha}$$

β increases by large amount for small increase in 'α'.

7.3.2. Reverse Current (I_{CBO} and I_{CEO}): [Leakage Current]

- The current I_{CBO} is the reverse current flowing from collector to base with emitter open circuit.
- The current I_{CEO} is the collector to emitter leakage current when base is open circuited.

Input	Output	Common Terminal
B	C	Emitter (Common Emitters)
B	E	Collector (Common Collector)
E	C	Base (Common Base)

For common base:

$$I_C = \alpha I_E + I_{CBO}$$
$$I_D = \beta I_S + (\beta+1) I_{CBO}$$

For Common Emitter:

$$\frac{I_E}{I_B} = \gamma \text{ common collector current gain factor}$$

$$I_E = v_{IB} \Rightarrow I_E = v\,(I_E - I_C)$$

$$\frac{I_C}{I_E} = \frac{\gamma - 1}{\gamma} = \alpha$$

$$\gamma = \frac{1}{1-\alpha} = 1 + \beta$$

Current gain contributing factors:

1. DC common base current gain:-

$$\alpha_0 = \frac{I_C}{I_E} = \frac{J_{nc} + J_G + J_{PCO}}{J_{nE} + J_{PE} + J_R}$$

where, J_{nC}: It is due to the diffusion of minority carrier $e^{\ominus}$ in the base at $x = x_b$

J_G : It is due to the generation of carriers in the R_B in the base – collector junction

J_{PCO}: It is due to the flow of minority carries in the R_B in the base collector junction

J_{nE} : due to diffusion of minority carries $e^{\ominus}$ in the base at x = 0

J_{PE} : due to diffusion of minority carrier hole in the base at x' = 0

J_R : due to recombination of carrier in the F_B base-emitter junction.

For AC sinusoidal i/p :

$$\alpha = \frac{\partial I_C}{\partial I_E} = \frac{J_{nC}}{J_{nE} + J_{PE} + J_R}$$

Change in I_C corresponding to change in I_f and J_G & J_{PCO} are independent of emitter current

$$s = \gamma \propto T^{\delta}$$

where, $\gamma = \frac{J_{nE}}{J_{nE} + J_{PE}} \rightarrow$ Emitter injection efficiency

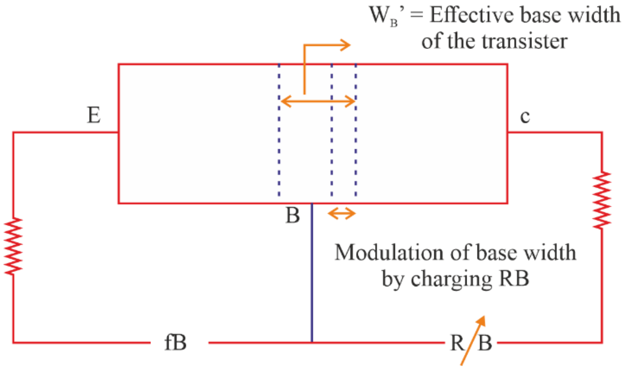
$$\alpha T = \frac{J_{nC}}{J_{nE}} \rightarrow \text{Base transport factor}$$

$$\delta = \frac{J_{nE} + J_{PE}}{J_{nE} + J_{PE} + J_R} \rightarrow \text{Recombination factor}$$

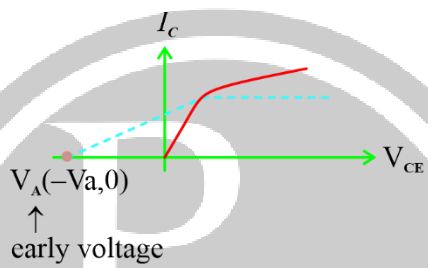
- α_T, γ & s are contributing factors, ideally all values are 1 but partially its close to 1.
- Distribution of minority carriers in npn transistor in forward active mode.

Base Width Modulation:

- The process where the effective base width of the transistor is altered by varying collector junction voltage is called base width modulating.
- It is also called as early effect



- As the base-callector RB voltage ↑es which reduced the neutral base width W'B by increasing the base, collector space charge region width.
- As W'B reduces, It will increase β
- The early effect produces a non-zero slope in o/p chrematistics & gives rise to a finite o/p conductance



Slope, $$g_0 = \frac{\partial I_C}{\partial V_{CE}}$$

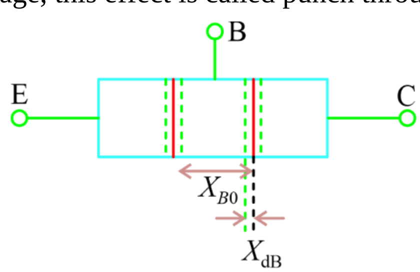
$$I_C = g_o (V_{CE} + V_A)$$

Where, $$g_0 = \frac{I_C}{V_{CE} + V_A}$$

7.3.4. Breakdown phenomena's in BJT

(1) Punch through breakdown:

- As the reverse bias base-collector voltage increases, the base-collector space charge region widens & enters further into the neutral base, It is possible for the base-collector depletion region to penetrate complete the base & reach the base emitter space charge region, the effect called punch through.
- The lowering of the potential barrier at the base-Emmiter junction, produces a large ↑ing current with the very small decreasing in the collector base voltage, this effect is called punch through breakdown phenomenan.



Let the depletion width for BE junction is negligible for breakdown
total neutral base width = X_{B0}

$$x_{dB} = x_{BO}$$

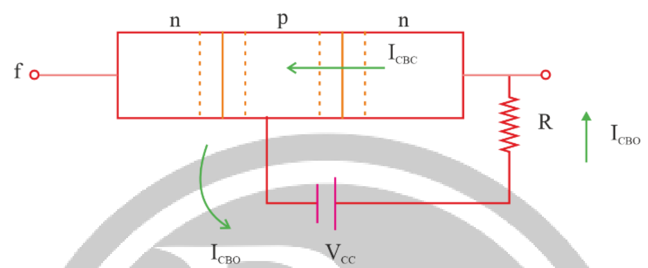
and, $$x_{dB} = \sqrt{\frac{2\varepsilon}{q}(v_{bi} + V_{CB}).\frac{N_C}{N_B} \times \left(\frac{1}{N_C + N_B}\right)}$$

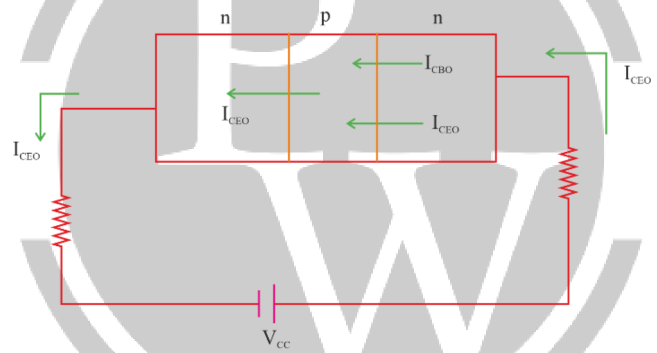
At break down :- $x_{dB} = x_{BO}$ & $V_{CB} = V_{PT}$ (negligible V_{bi})

Then, $$V_{PT} = \frac{x_{dB}^2 q N_B (N_C + N_B)}{2\varepsilon N_C}$$

(2) Avalanche Breakdown:

- When a high reverse voltage is applied across the diode then avalanche breakdown takes place.
- When emitter is open then current (I_{CBO}) will flow from the collector to base & then by V_{CC} by applying V_{CC}.



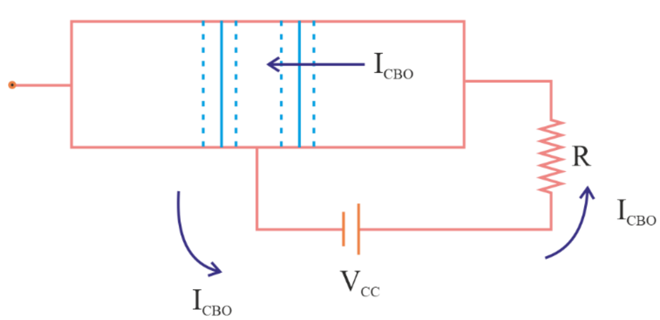


In B – C RB minority carrier of collector will flow to base then base will positively charged the E – B is FB.

$$I_{CEO} = I_{CBO} + \alpha I_{CEO}$$

$$I_{CEO} = \frac{I_{CBO}}{I - \alpha} \Rightarrow I_{CEO} = (1 + B)I_{CBO}$$

$$\boxed{I_{CEO} = (1+\beta)I_{CBO}}$$



Breakdown occurs when $I = MI_{CBO}$

Where, M → multiplication factor

Empirical formula for M

$$M = \frac{1}{1-\left(\frac{V_{CB}}{BV_{CBO}}\right)^n}$$

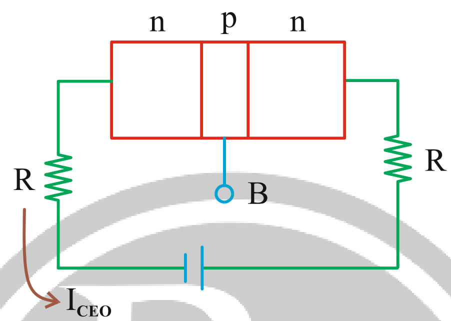
Where, $BV \rightarrow$ breakdown voltage

$n \rightarrow$ emphatical constant

BV_{CBO} = Breakdown voltage (V_{CB}) in open Emitter configuration

i.e For Breakdown $V_{CD} = BV_{CBO}$

7.3.5. In Open Base Configuration



$$I_{CEO} = M[I_{CBO} + \alpha I_{CEO}]$$

$$I_{CEO} = \frac{M}{1-M\alpha} \cdot I_{CBO}$$

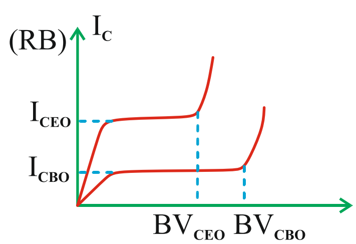
For B.D : $M = 1$

$$M = \frac{1}{1-\left(\frac{V_{CB}}{BV_{CBO}}\right)^n}, \text{ at } V_{CB} = V_{CE} \quad M = \frac{\alpha}{1-\left(\frac{BV_{CEO}}{BV_{CB}}\right)^n} = 1$$

$$BV_{CEO} = BV_{CB}(1-\alpha)^{1/n}$$

$$BV_{CEO} = \frac{BV_{CEO}}{(\beta)^{1/n}}$$

The breakdown voltage in the open base configuration is smaller then the actual avalanche junction breakdown voltage.



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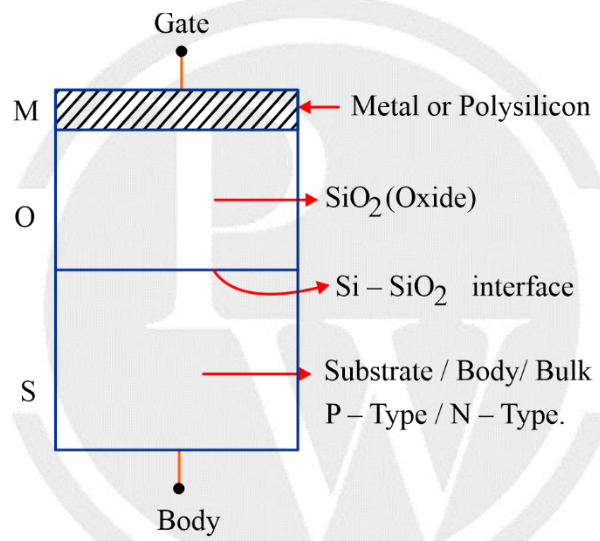
8 MOS CAPACITOR

8.1. MOS Capacitor

MOS → Metal oxide semiconductor

Oxide used is (SiO_2) →Insulator.



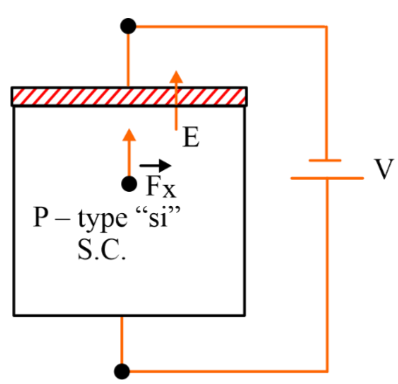
MOS capacitor Operates in 3 – modes:

(1) Accumulation.

(2) Depletion.

(3) Inversion.

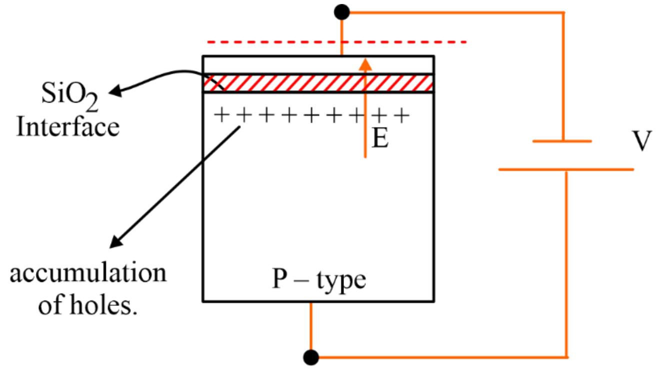
(1) Accumulation.



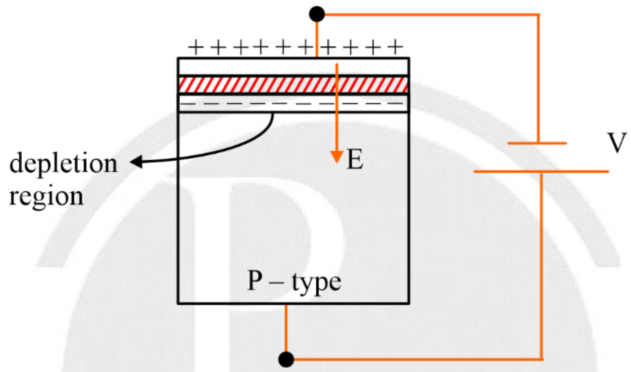
This E field is very strong so that it penetrates in p – type S.C.

Also, the holes of S.C. P – type get forced and accumulate at surface.

(2) Depletion mode:



(3) Inversion Process:



Inversion process:

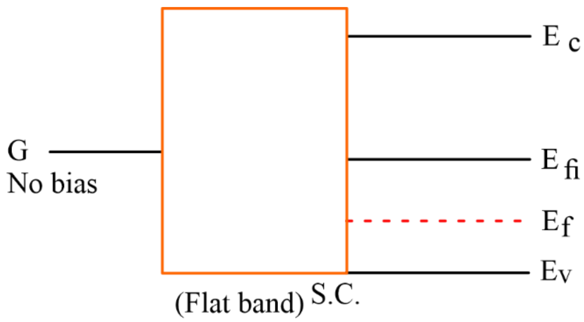
- In this on metal the ions are there and in p – type holes are forced in the direction of $\vec{E}$ field and this is created a depletion region.
- When a MOS capacitor with a p-type SC substrate is biased such that the top metal gate is at a (–ve) voltage w.r.t. the S.C. substrate.
- An accumulation layer of hole is created at the oxide S.C. interface corresponds to the (+V) charge on the bottom plate of the MOS capacitor.

Strong Inversion

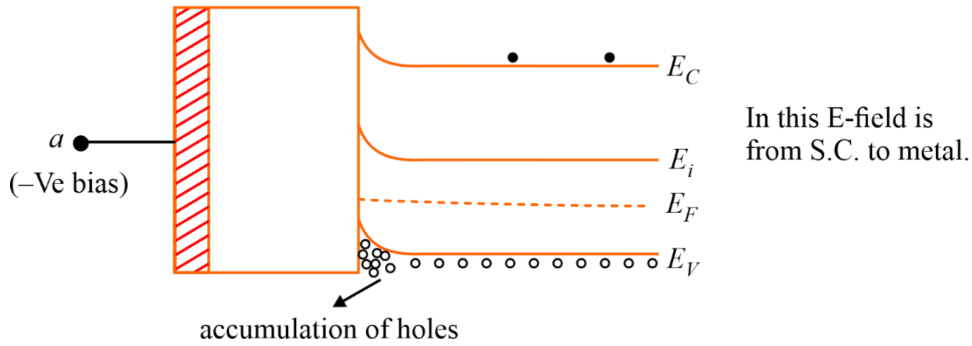
- Now consider the same MOS capacitor in which the polarity of applied voltage is opposite of 1'st case.
- A positive case charge exists on the top' of metal plate and the induced E-field is in the direction from metal to S.C.

Energy Band Diagram: (p-type S.C substrate)

(1) No gate bias:

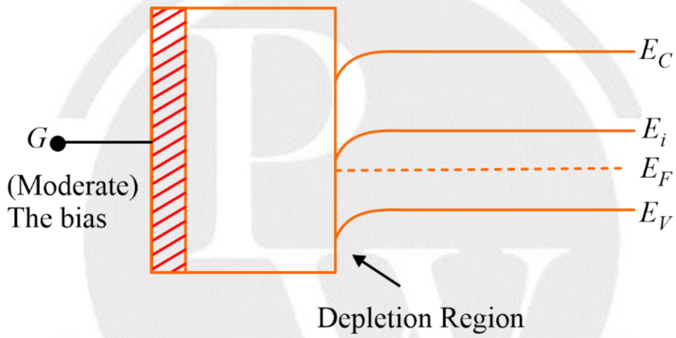


(2) Gate at Negative Voltage:



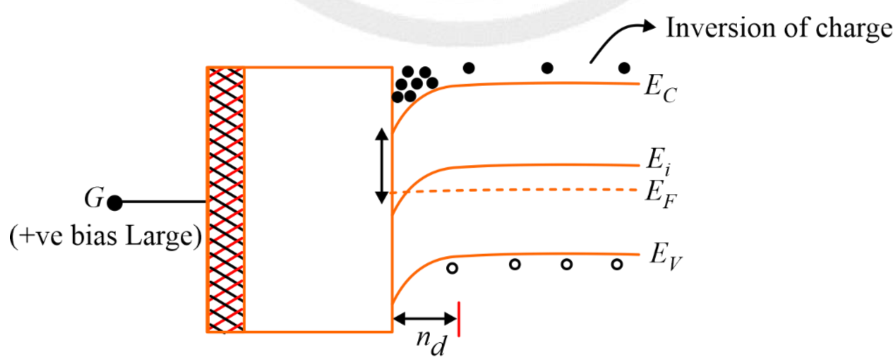
- Here, V_B is more nearer to fermi level than bulk so it is more p-type surface then bulk.
- "E_f" is constant, because it is in thermal equilibrium.

(3) Gate at positive voltage: (moderate)



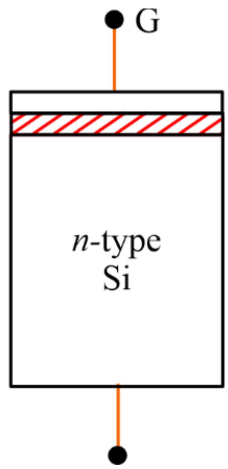
- In this case bulk is more p-type then surface and holes are depleted towards bulk and there is depletion region at surface. (Thermal equilibrium is also there) surface starts to become n-type.

(4) Inversion:

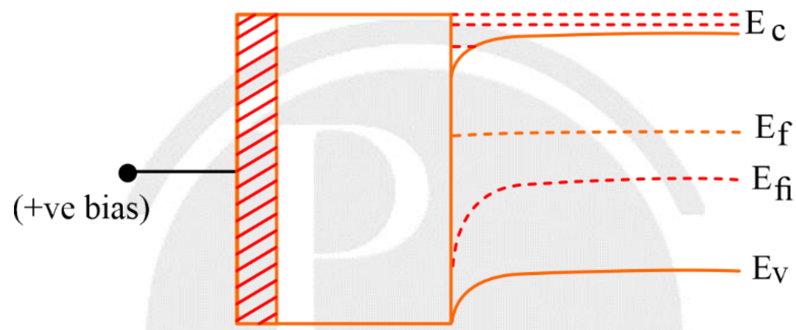


- – ve charge in a MOS capacitor implies a larger induced space charged region and more bonding
- The intrinsic fermi level at the surface is now below the fermi level.

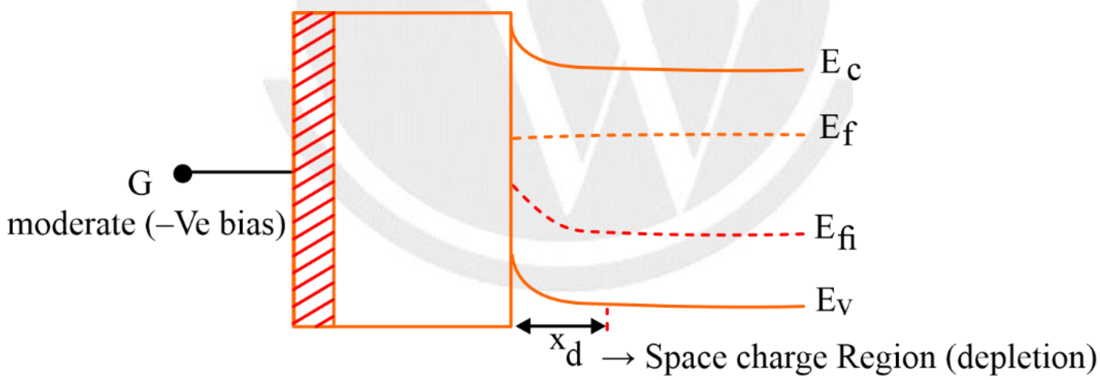
n-type: (Energy Band diagram)



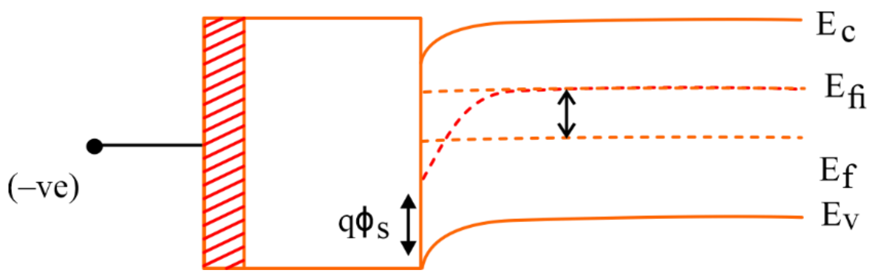
(1)



(2)



(3)



ϕs = surface potential

$q\phi_s = E_{fi}$ Bulk – E_{fi} surface.

- At inversion point ➔ Surface is as much n-type as bulk is p-type.

$$n = N_c\, e^{-\left(E_c - E_f\right)/KT} = n_i\, e^{-\left(E_{fi} - E_f\right)/KT}$$

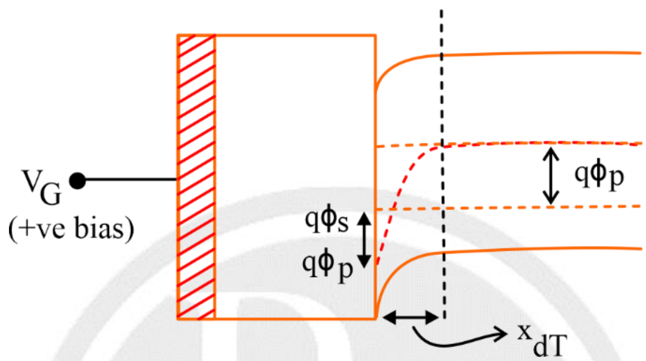
$$p = N_v e^{-(E_f - E_v)/KT} = n_i \, e^{-(E_f - E_{fi})/KT}$$

Electron concentration at bulk S.C.

$$p_e = N_i \, e^{-(E_f - E_{fi})/KT}. \qquad \text{for } n_s = p_B$$

$$\left[E_{fis} - E_f = E_f - E_{fiB}\right] \rightarrow \text{inversion}$$

for Inversion: $\phi_s = 2\phi_{fp}$



Maximum depletion region thickness.

$$\phi_{fp} = V_T \ln\left(\frac{N_A}{n_i}\right)$$

$N_A \longrightarrow$ Acceptor concentration in p-type substrate.

$\phi_s \longrightarrow$ surface potential (potential deft. Across depletion region)

$$x_d = \left(\frac{2\varepsilon}{q}\frac{\phi_s}{N_A}\right)^{1/2} \longrightarrow \text{Like a one sided.}$$

Maximum depletion region width occurs at

$$\phi_s = 2\phi_{fp}.$$

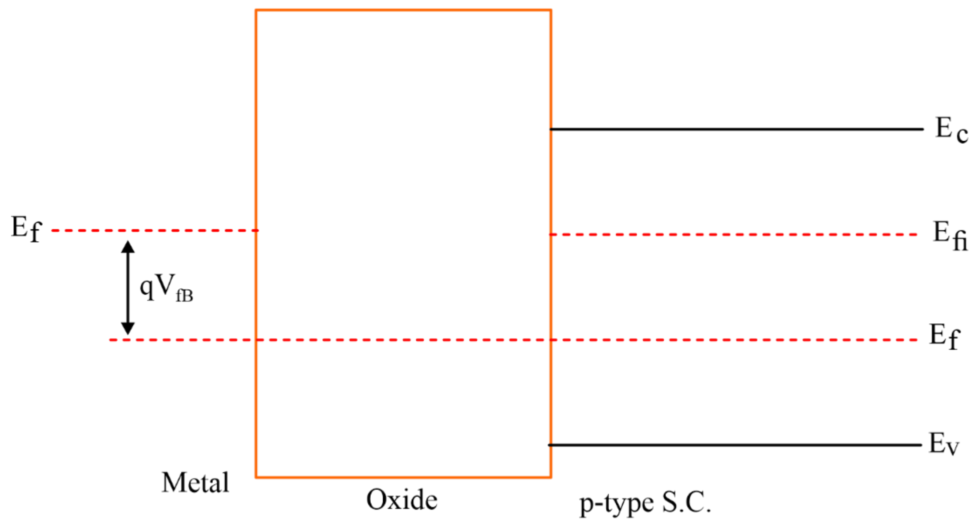
$$x_{dT} = \left(\frac{4\varepsilon\phi_{fn}}{q\, N_D}\right)^{1/2}$$

$$\phi_{fn} = V_T \ln\left(\frac{N_D}{n_i}\right)$$

- At the surface, potential $\phi_s = 2\phi_{fp}$
- The fermi level at the surface is as for above the intrinsic level in the bulk S.C.
- This condition is known as the 'threshold inversion point'.
- The applied gate voltage operating this condition is known as the threshold voltage.

Flat Band Voltage:

This is a applied gate voltage such that is no band bending in the S.C. and as a result there is zero net space charge in this region.



$$V_G = \Delta V_{ox} + \Delta\phi_s$$

At flat – Band, $V_G = V_{FB}$

$$V_{FB} = (V_{ox} - V_{oxo}) + (\phi_s - \phi_{so})$$

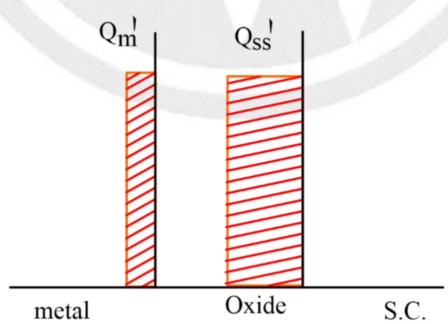
We know: $(V_{oxo} - \phi_{so}) = \phi_{ms}$

$$V_{fB} = \phi_{ms} + V_{ox} + \phi_s$$

Also, at flat bond $\phi_s = 0;$

$$V_{fB} = \phi_{ms} + V_{ox}.$$

Charge distribution in MOS cap at FB voltage



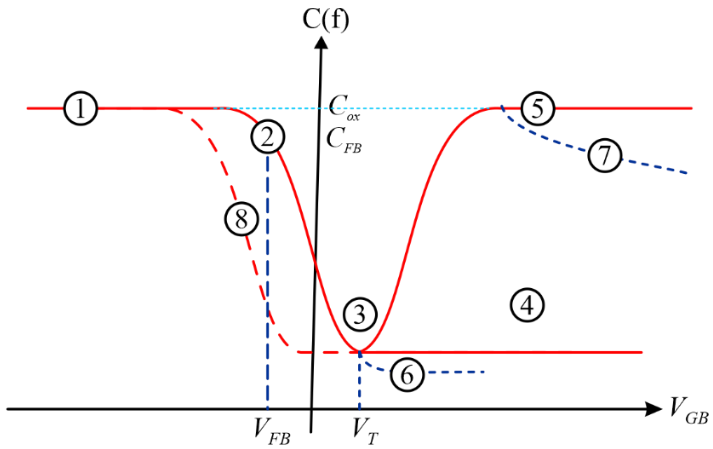
For conservation of charge:

$$\phi_m' + Q_{ss}' = 0 \quad ; \quad Q_m' = -Q_{ss}'$$

Across oxide voltage drop = V_{OX} → Voltage drop across capacitance.

$$V_{ox} = \frac{Q_m'}{C_{ox}} = \frac{-Q_{ss}'}{C_{ox}}$$

$$V_{FB} = \phi_{ms} + \frac{-Q_{ss}'}{C_{ox}}$$



① Accumulation
② Flat band
③ Inversion Start
④ High Frequency
⑤ Low Frequency
⑥ Deep Depletion
⑦ Poly Depletion Effect
⑧ Positive Oxide Charges Introduced

$V_{fB} \longrightarrow$ flat Band voltage.

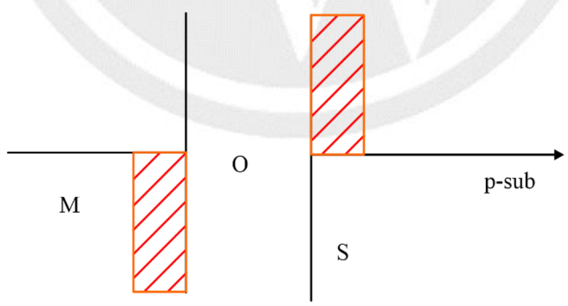
$V_G \longrightarrow$ Gate Voltage.

$V_T \longrightarrow$ Threshold voltage.

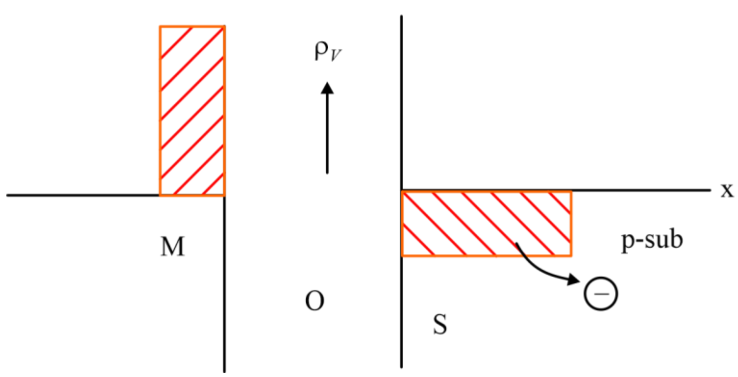
MOS Capacitor can operate in 3-modes Accumulation, Depletion, Inversion, which is explained earlier.

$$V_T = \pm Q_{msi} \pm \frac{Q_{ox}}{C_{ox}} \pm \frac{Q_d}{C_{ox}} \pm 2\phi_f$$

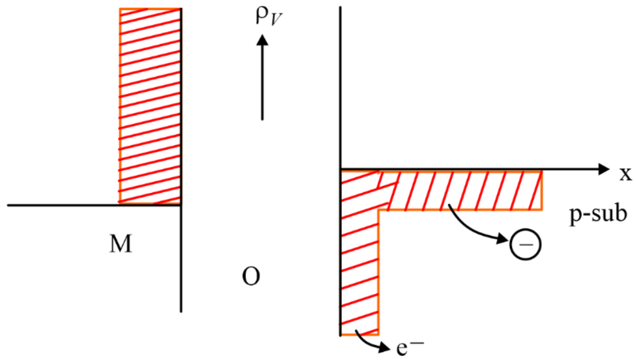
(I) Accumulation



(II) Depletion



(III) Inversion



Boundary Condition:

$$\bar{D}_{N_1} = \bar{D}_{N_2}$$

$\Rightarrow$ $$\epsilon_{ox} E_{ox} = \epsilon_{si} E_s$$

Where, $\epsilon_{si} = 11.7\epsilon_o$

$\epsilon_{ox} = 3.9\epsilon_o$

Then, $$E_s = \frac{\epsilon_{ox}}{\epsilon_{si}} E_{ox}$$

$$\bar{E}_{ox} = \frac{|Q_s|}{\epsilon_{ox}} c/cm^2$$

$$\bar{E}_s = \frac{|Q_s|}{\epsilon_{si}} c/cm^2$$

$$E_s = \frac{2\phi_s}{w_d}$$

$$V_{ox} = E_{ox} t_{ox}$$

Flat band capacitance:

$$C_{FB} = \frac{1}{\frac{1}{C_{ox}} + \frac{L_D}{\epsilon_s}}$$

L_D = Debye length

$$L_D = \sqrt{\frac{\varepsilon_S \phi_t}{qN_A}}$$

$\phi_t \rightarrow$ Thermal voltage

$$C'_{FB} = \frac{\varepsilon_{ox}}{t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_s}\sqrt{\frac{\varepsilon_s \phi_t}{qN_A}}} \text{ F/cm}^2$$

The flat band capacitance of the MOS structure at flat band is obtained by calculating the series connection of the oxide capacitance and the capacitance of the semiconductor

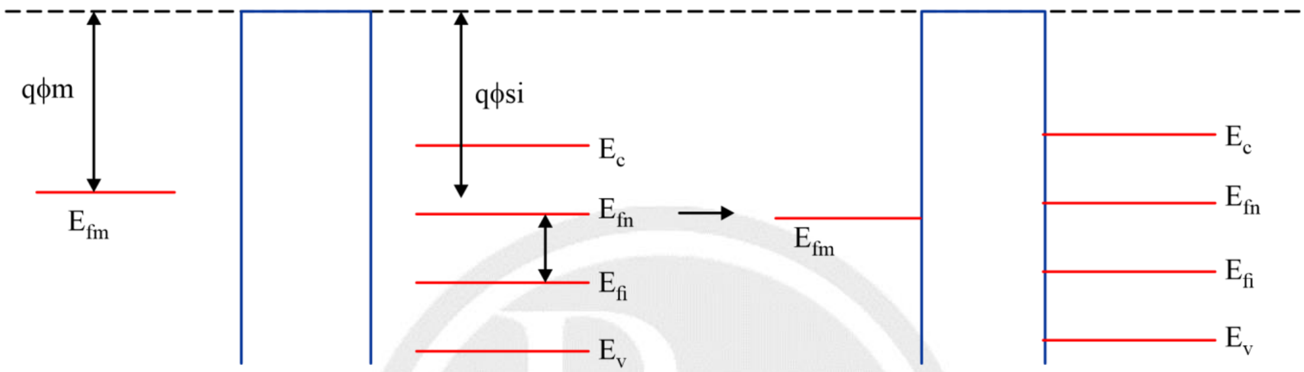
Energy Band Diagram:

For N-sub MOS capacitor:

Ideal case: (1) $\phi_m Si = 0$

(2) $Q_{ox} = 0$

(i) Flat band: ($V_G = 0$)



(ii) Accumulation → $V_G > 0$

(iii) Depletion mode $V_G < 0$

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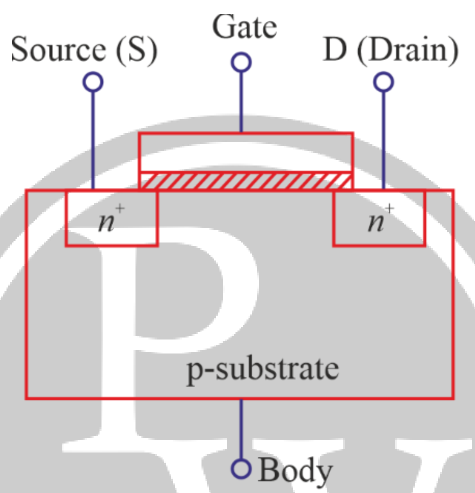
9 MOSFET
(Metal Oxide Semiconductor Field Effect Transistor)

9.1. MOSFET



- **Source :** terminal through which majority charge carrier enters into the SC bar.
- **Drain :** terminal through which majority charge carriers leaves the SC bar.
- **Channel:** path between source & drain by which majority carrier travel from source to drain
- **Gate :** Terminal to control the flow of charge carrier from source to drain

MOSFET

Enhancement type MOSFET

- No initial channel between 'S' & 'D' at zero gate voltage

(a) *n* - channel (N-mos)

(b) *p* - channel (P-mos)

Depletion type MOSFET

- Channel is initially present in between 'S' & 'D' at zero gate voltage

(a) *n* - channel

(b) *p* - channel

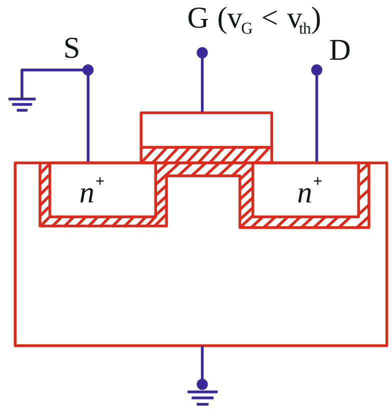
- Depletion type MOSFET, the already created channel is either of following two types

  (i) Internally doped

  (ii) A mos device with applied threshold voltage.

9.2. Operation of Enhancement Mode N-MOS :

(I)

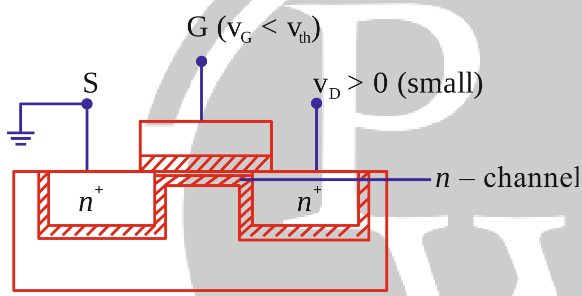


- There is no flow of 'S' carrier to drain

  Here, v_{th} = threshold voltage +ve for N-channel MOS

  –ve for P-channel MOS

(II)



- Source carrier (e^-) will flow from S to D, therefore channel & a current will flow from 'D' to 'S'
- For small V_D, $\boxed{I_{DS} = g_d v_{DS}}$

  $g_d \propto |Q_n'|$, where $Q_n \rightarrow$ Inversion charge

  $$\boxed{|Q_n'| \propto v_{ox} - v_{th}}$$

  Potential difference across oxide layer

  $$|Q_n'| = \left[v_{GS} - v_{(x)} - v_{TH}\right]$$

  Where, $v_{(x)} \rightarrow$ potential at any point in channel at source : $x = 0$

  $$v_{(o)} = ov$$

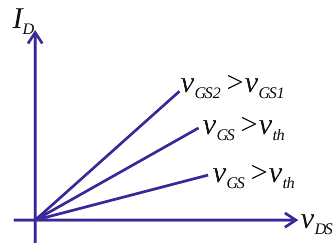
  and $v_{(L)} = v_{DS}$ $\left(o \le v_{(x)} \le v_{DS}\right)$

- For v_{DS} very small

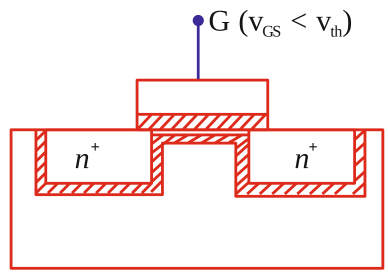
  $$\boxed{v_{ox} \simeq v_{GS} - v_{TH}}$$

  Then $|Q_n'| \propto v_{GS} - v_{TH}$

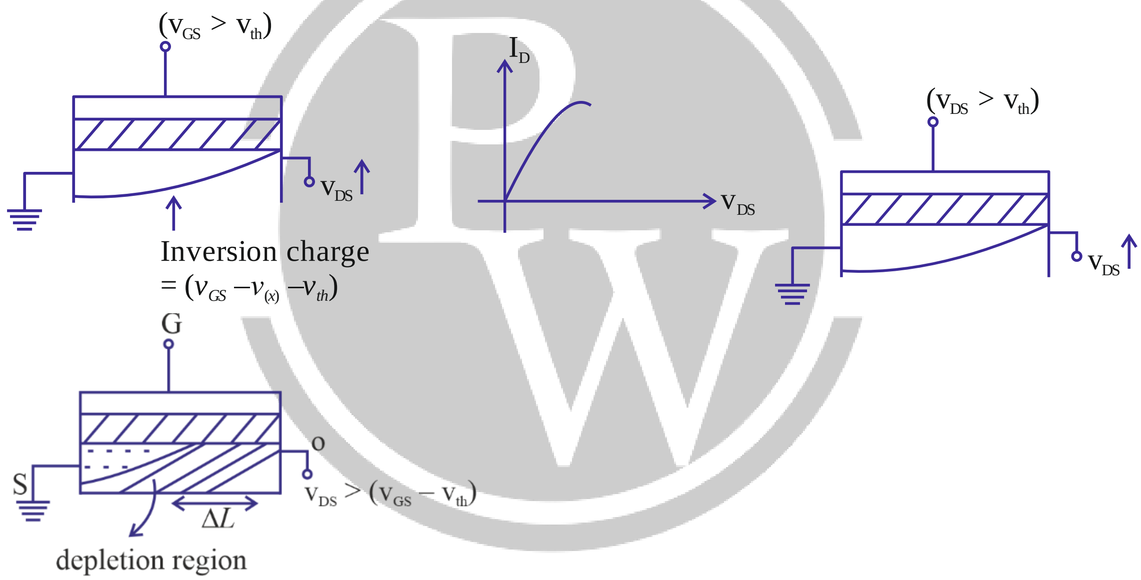
  $\boxed{g_d \propto v_{GS}} \rightarrow$ Basic MOSFET action (modulation of channel cond by applying gate val)

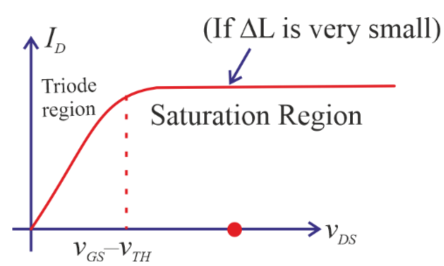


(III)



- At small $v_{DS}, |Q_n'| \propto v_{GS} - v_{TH}$
- Inversion charge density at the channel, *i* const.





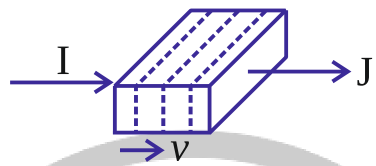
For $v_{GS} > v_{TH}$:

- For small value of v_{DS} the charge density is const along the entire channel length therefore drain current ↑es linearly with v_{DS}.
- If v_{DS} ↑es, the voltage drop across one oxide layer near the drain terminal decreases, which means the incremental conductance of the channel at the drain decreases which means slope of I_D vs V_{DS} will decreases
- When v_{DS} increase to $(v_{GS} - v_{TH})$ then the slope of I_D v/s v_{DS} curve will zero.

9.2.1. In depletion mode MOSFET

- If the n-channel region is actually induced an inversion layer of e^- created by the metal SC work function diff. & the fixed charge in the oxide, the current voltage characteristics is same as above, only except v_{th} is negative quantity.
- If the n-channel region is actually an n-type SC region & Q –*ve* gate voltage will induced a depletion region under the oxide, reducing the thickness of the n-channel region, reduced thickness decreases the channel conductance which reduces the drain current.
- In order to be able of to turn the device off, the channel thickness must be less than the maximum charge width (xdT)

Derivation of I-V characteristics :

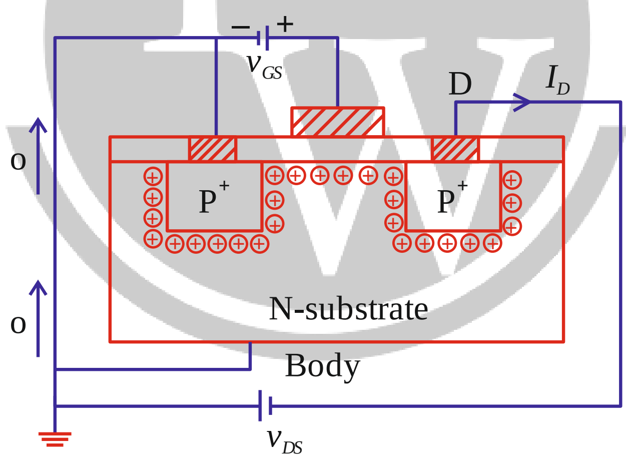


$Q_d \rightarrow$ Charge carrier/length along the direction of flow of current

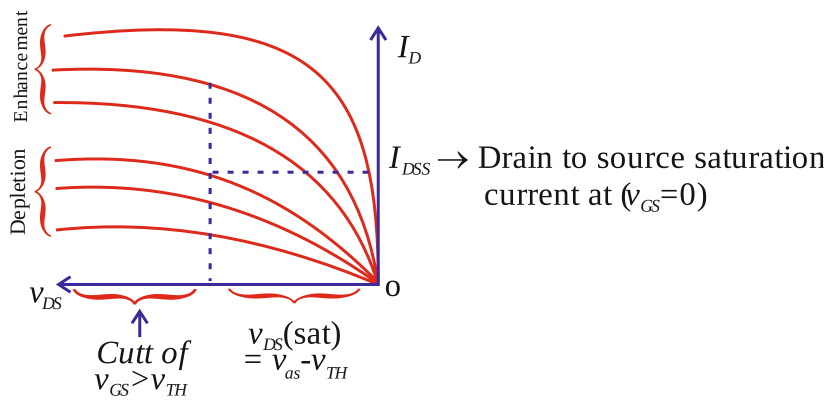
$v \rightarrow$ Velocity of charge carrier

Total charge = Qdv

P-channel Depletion Type MOSFET :



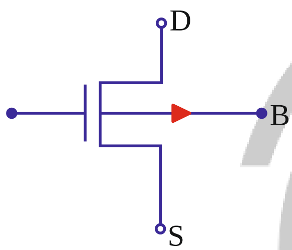
Output Characteristic :



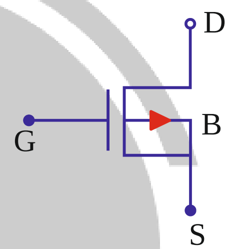
- If $v_{GS} > 0$ & v_{DS} (vary)
  - Depletion charge Q_D increases
  - Less holes available in channel i.e. I_D decrease
  - Channel depleted
- If $V_{GS} < 0$ & V_{DS} (vary)
  - Depletion charge Q_b in creases
  - More holes available i.e. I_D will increases
  - Channel – Enhance
- In linear region :

$$\boxed{I_D = \frac{1}{2}\mu_n Cox\left(\frac{W}{L}\right)(v_{GS} - v_{TH})^2}$$

Symbol :



or



- N-channel Enhancement type MOSFET :

$$\boxed{I_D = \frac{1}{2}\mu_n Cox\frac{W}{L}\left[(v_{GS} - v_{TH})v_{DS} - \frac{v_{DS}^2}{2}\right]}$$

MOSFET works as voltage variable resistor

Trans Conductance :

- It is a figure of merit indicates that how well a transistor convert the voltage to the current

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{V_{DS} = \text{const.}}$$

- In triode region :

$$\frac{\partial I_D}{\partial V_{GS}}\bigg|(V_{DS} = \text{const.}) = g_m = \mu_n Cox\frac{W}{L}v_{DS}$$

- In saturation region :

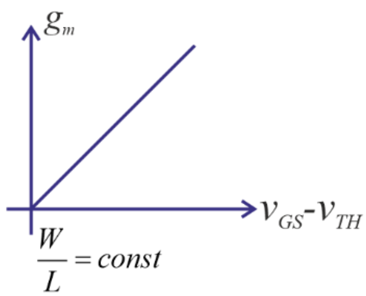
$$v_{DS} = v_{GS} - v_{TH}$$

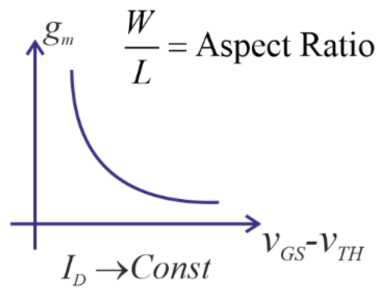
$$\boxed{I_{D\,\text{sat}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[v_{DS} - v_{TH}]^2}$$

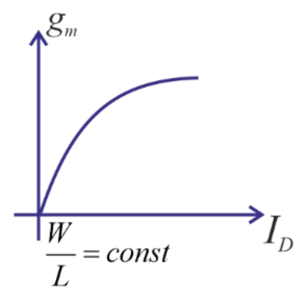
and $$g_m = \mu_n C_{ox}\frac{W}{L}[v_{GS} - v_{TH}]$$

$$g_m = \frac{2I_{D\,sat}}{v_{GS} - v_{TH}}$$

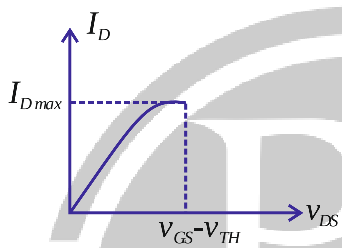
$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)I_D}$$







- When, $v_{DS} < v_{GS} - v_{TH}$ (the Triode region)



$v_{GS} < v_{TH} = v_{ov}$ (over drive voltage)

- The channel is pinched off at $v_{DS} = v_{ov}$. The drain current reaches its maximum value & if we further increases v_{DS}, a const current flow because of the pinched off channel side $Q_d \rightarrow o$ & velocity of carrier increases.

In triode Region :

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(v_{GS} - v_{TH})v_{DS} - \frac{v_{DS}^{\ 2}}{2}\right]$$

Let $2(v_{GS} - v_{TH}) >> v_D$

Then it is deep triode region $\Rightarrow$ Linear Region

$$I_D I \cdot \mu_n C_{ox}\frac{W}{L}(v_{GS} - v_{TH})v_{DS}$$

$$I_D \propto v_{DS} \Rightarrow I_D = g_d v_{DS} \text{ (channel conductivity)}$$

$$\boxed{g_d = \mu_n C_{ox}\frac{W}{L}(v_{GS} - v_{TH})}$$

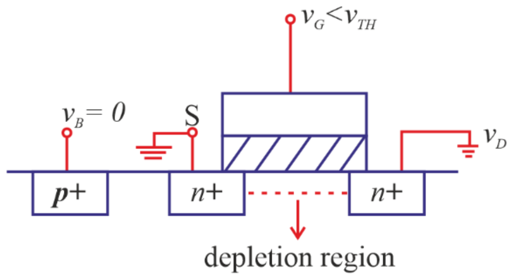
$$\boxed{R_{CH} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(v_{GS} - v_{TH})}}$$

In deep triode region MOSFET work as a linear resistor which can be varied by v_{GS} therefore in deep triode region, we can say that it is working as a voltage variable resistor.

2nd order effects :

1. Body - Bias effect : (N-MOS)

- If $v_B < 0$



Then, attracts more holes towards body terminal hence depletion charge increase before on set of inversion.

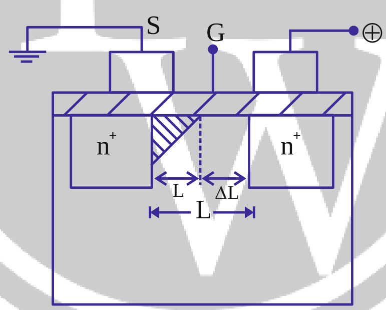
- The gate charge must mirror Q_d before an inversion layer is formed. Therefore, v_{GS} is a function of total charge in depletion region.
- If v_B is increased, then Q_o will increase and then v_m will increase

$$v_{TH} = v_{THo} + \gamma\sqrt{2C_{ox}{}^{+}v_{SB}} - \sqrt{2\phi_F}$$

$$\boxed{v = \frac{\sqrt{2 \in qN_{sub}}}{C_{ox}}}$$

Body effect coefficient

2. Channel length Modulation:



Where, L $\rightarrow$ Actual length of channel

ΔL $\rightarrow$ Depleted channel length

L' = L – ΔL $\rightarrow$ Un-depleted length or effective channel length

$$\boxed{I_D = \frac{1}{2}\mu_n Cox\left(\frac{W}{L}\right)(v_{GS} - v_{TH})^2\left[1 + \lambda\left[v_{DS} - v_{DS}(sat)\right]\right]}$$

If $v_{DS} >> v_{DS(sat)}$

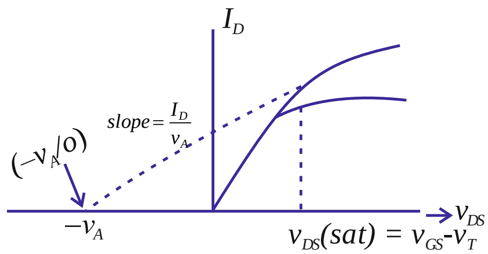
$$\boxed{I_D = \frac{1}{2}\mu_n Cox\left(\frac{W}{L}\right)(v_{GS} - v_{TH})^2\left[1 + \lambda v_{DS}\right]}$$

Where, $\lambda \rightarrow$ channel length modulation parameter

unit = volt^{-1}

$$\boxed{\lambda = \frac{1}{v_A}(\text{volt}^{-1})}$$

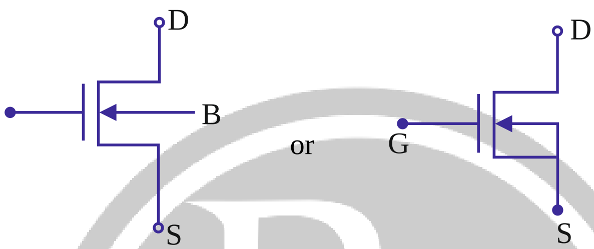
Where, $v_A \rightarrow$ Early voltage



- r_o (or) $\qquad rd = \frac{1}{slope} = \frac{v_A}{I_D} = \frac{1}{\lambda I_D}$

$$\boxed{r_o = \frac{1}{\lambda I_D} = \frac{v_A}{I_D}}$$ output resistance

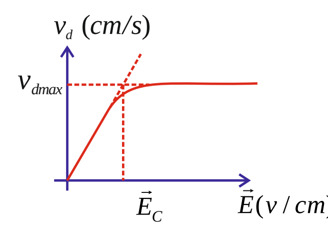
- Symbol N-channel enhancement type (NMOS) :



9.3. Short Channel Effects

The MOSFET is consider to be short channel device when the channel length is in the same order of the depletion width of source and drain junction.

1. Velocity Saturation
2. Drain-induced barrier lowering (DIBL)
3. Impact Ionization
4. Hot electron



$\vec{E}_C \rightarrow$ Critical Electric Field

1. Velocity Saturation:

By using previous study we can state:

$$v_d = \mu\vec{E}\left(\vec{E} << \vec{E}_C\right)$$

$$v_d = v_{d\max}\left(\vec{E} >> \vec{E}_C\right)$$

But the variations in v_d near the critical $\vec{E}$ field cannot be modelled using the above equation. This is the region in which v_d changes with $\vec{E}$, sub linearly.

Proposed model for velocity saturation.

$$\boxed{v_d = v_{d\max}\frac{\vec{E}/\vec{E}_C}{1+\frac{\vec{E}}{\vec{E}_C}}\text{ cm/s}}$$

This model gives the actual v_d versus $\vec{E}$.

2. Drain Induced Barrier Lowering

When we apply positive voltage at the drain in n-channel MOSFET having short channel, then its threshold voltage (v_T) will decrease due to depletion region of drain region. This effect can be reduce by increasing substrate doping.

3. Impact Ionization

In short channel devices the $\vec{E}$ field in the channel will be high and due to that the e^- velocity will be high which impact on Si atoms and generate electron hole pair, this is called as impact Ionization.

4. Hot Electron

This is also due to high $\vec{E}$ field in the channel which give rise to high energy of e^- and that can enter into the oxide and will be treated as trapped oxide charge. This will increase the threshold voltage (v_T).

❑❑❑